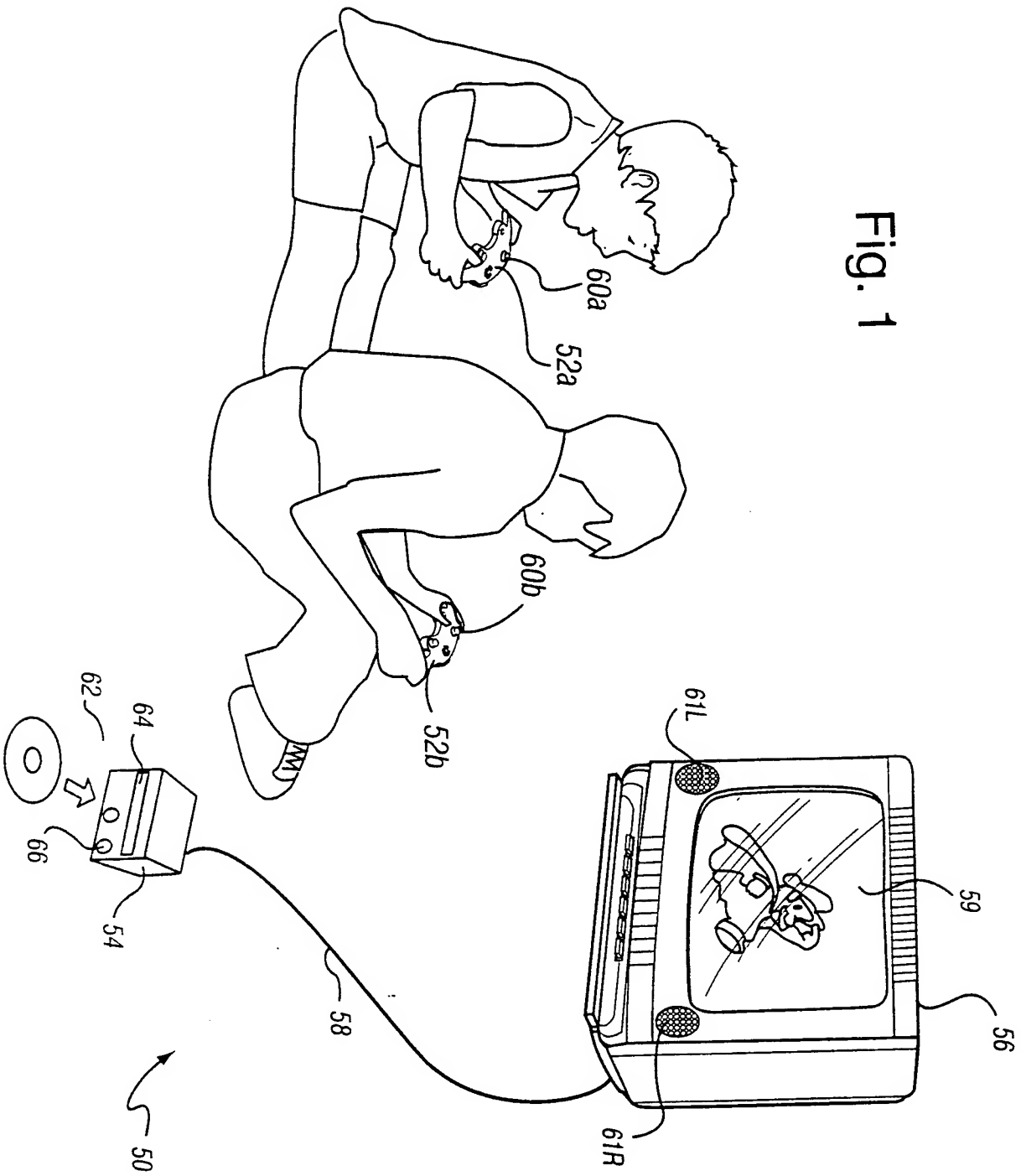


Fig. 1



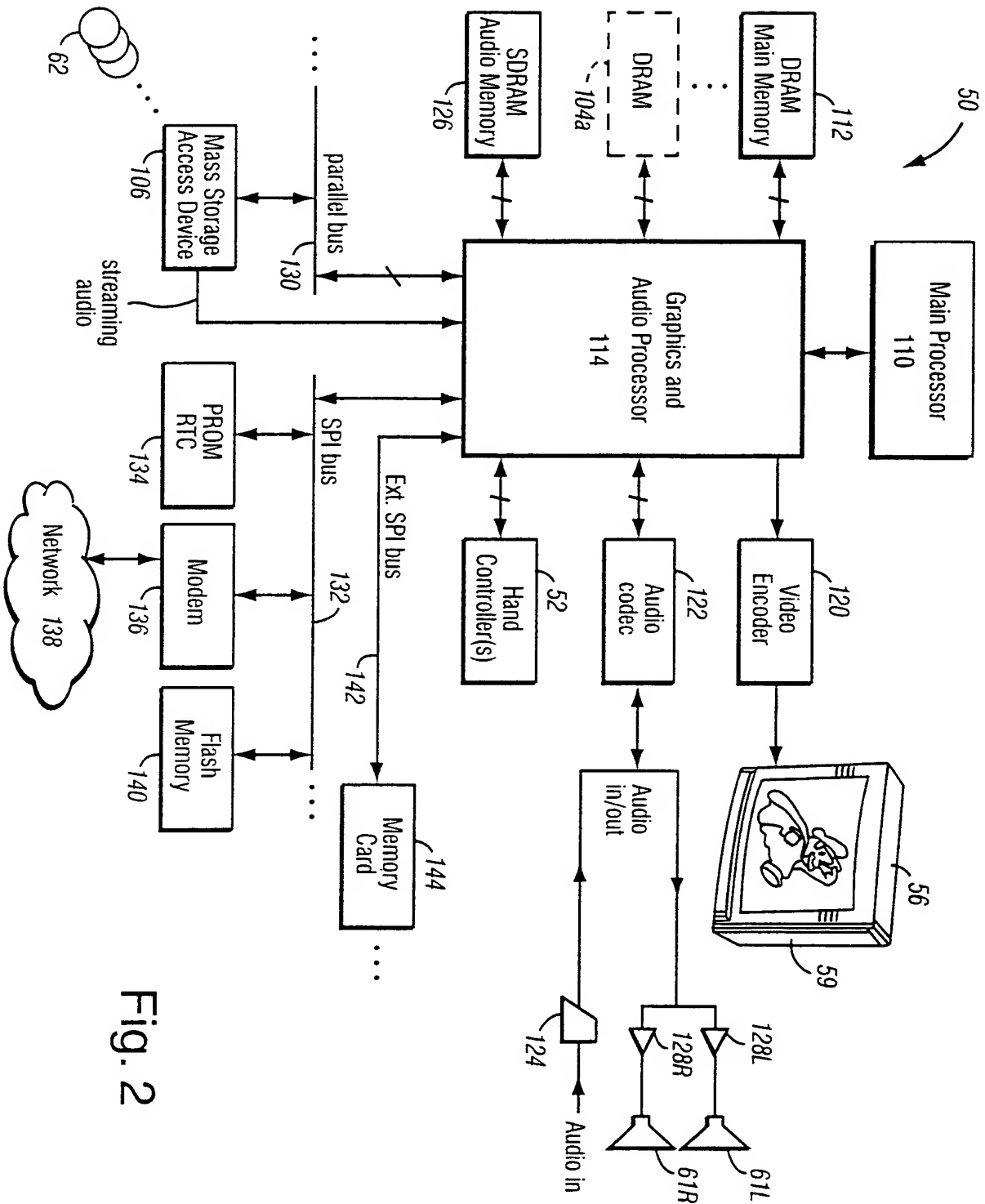
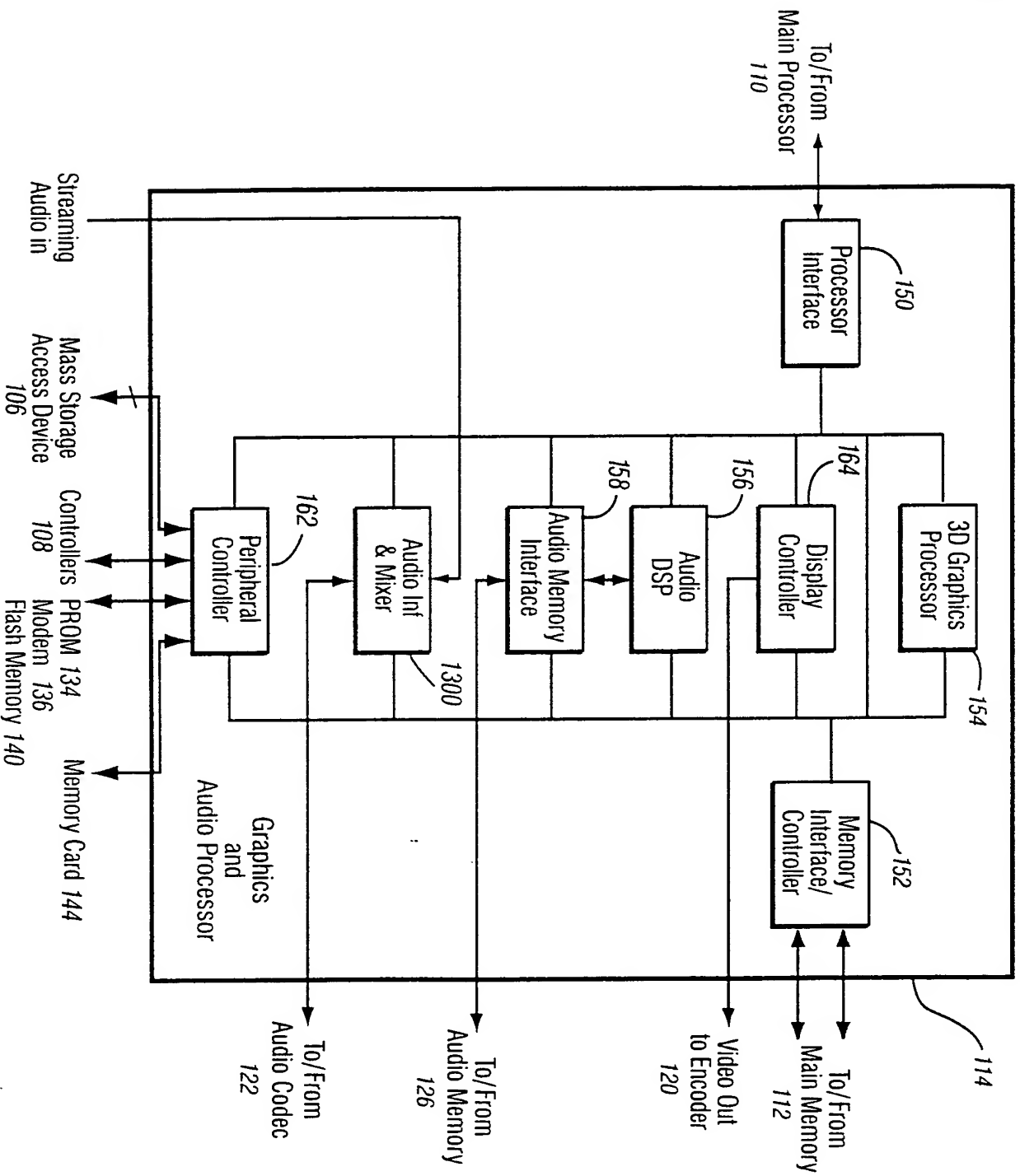


Fig. 2

Fig. 3



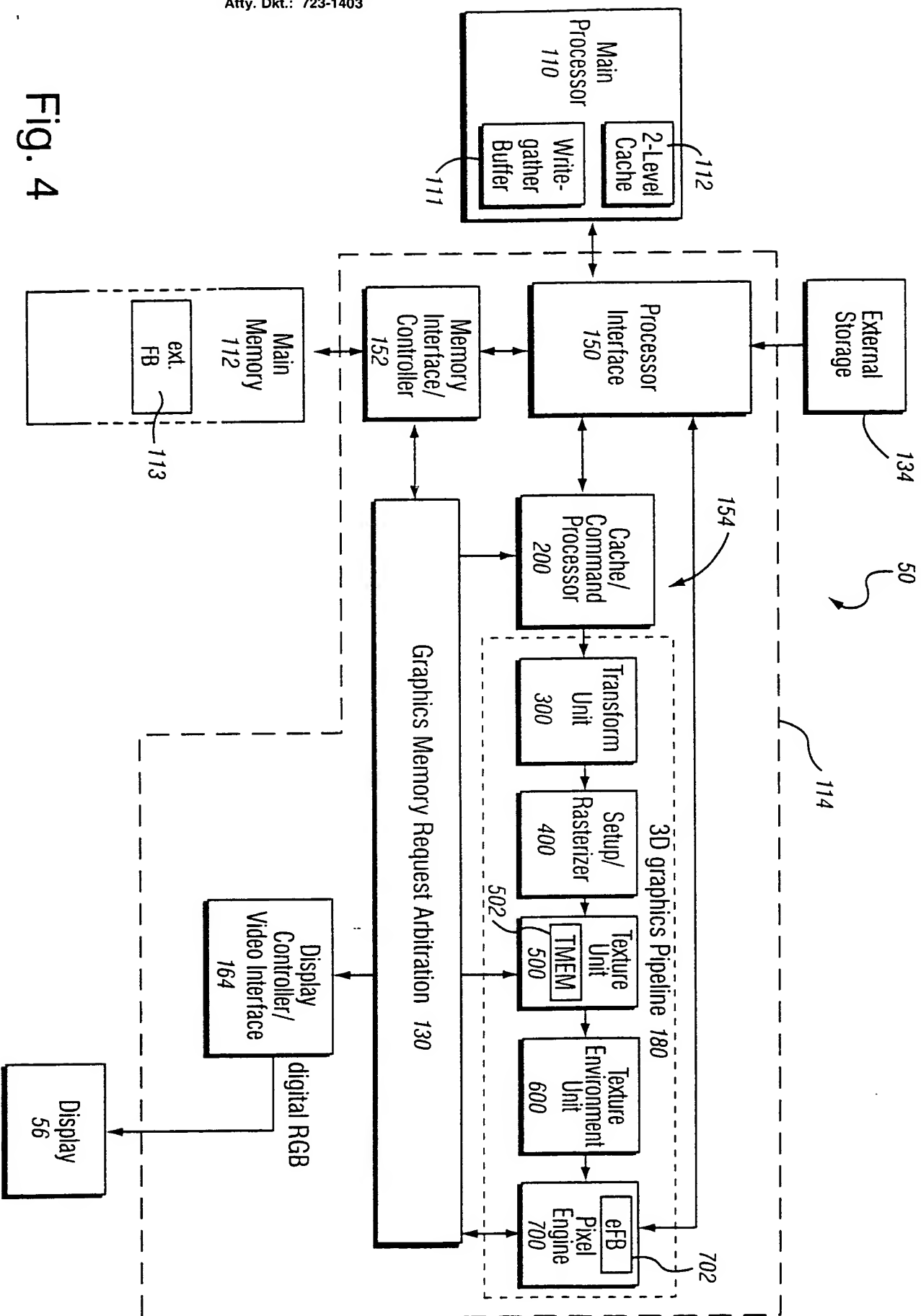


Fig. 4

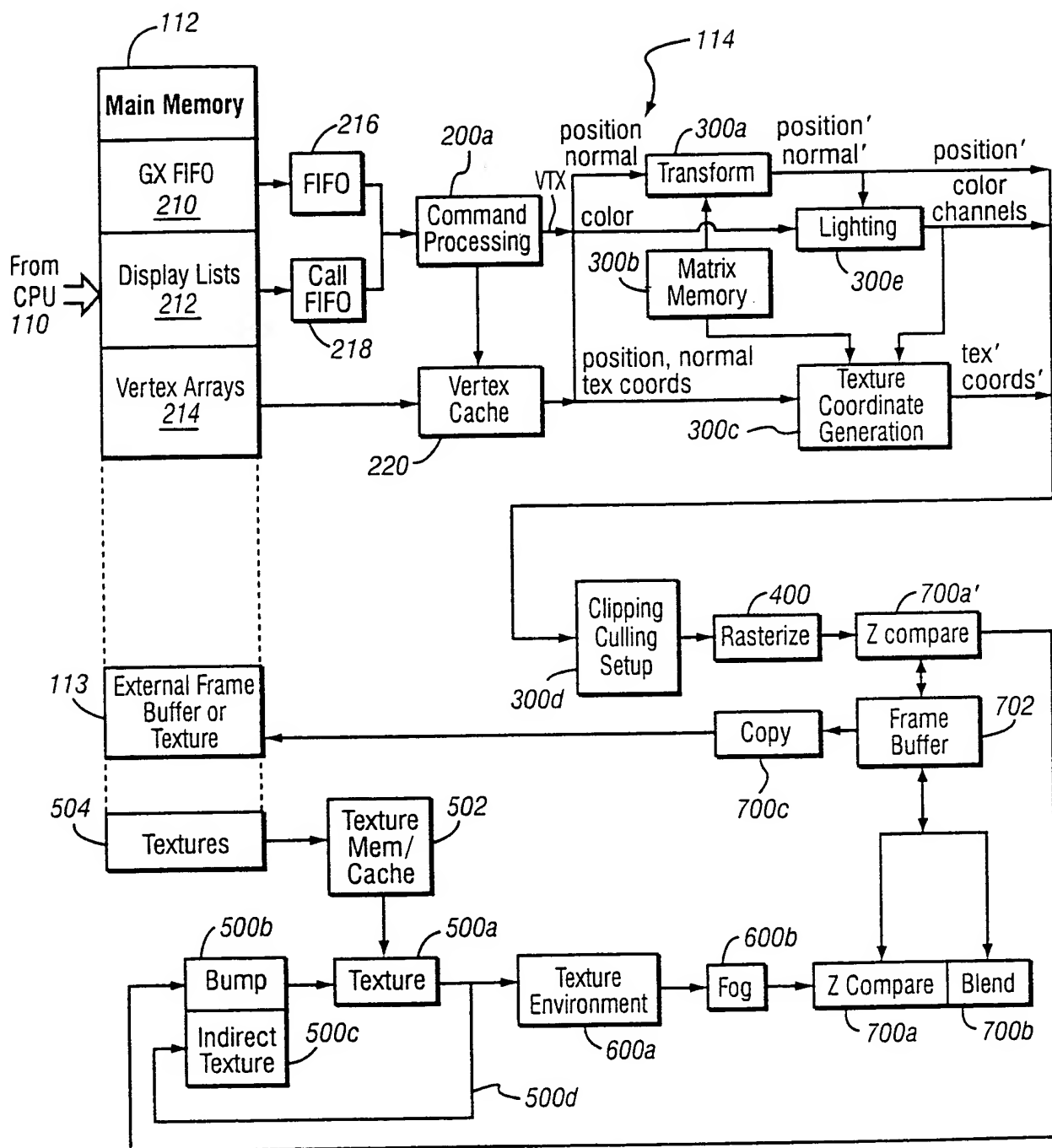
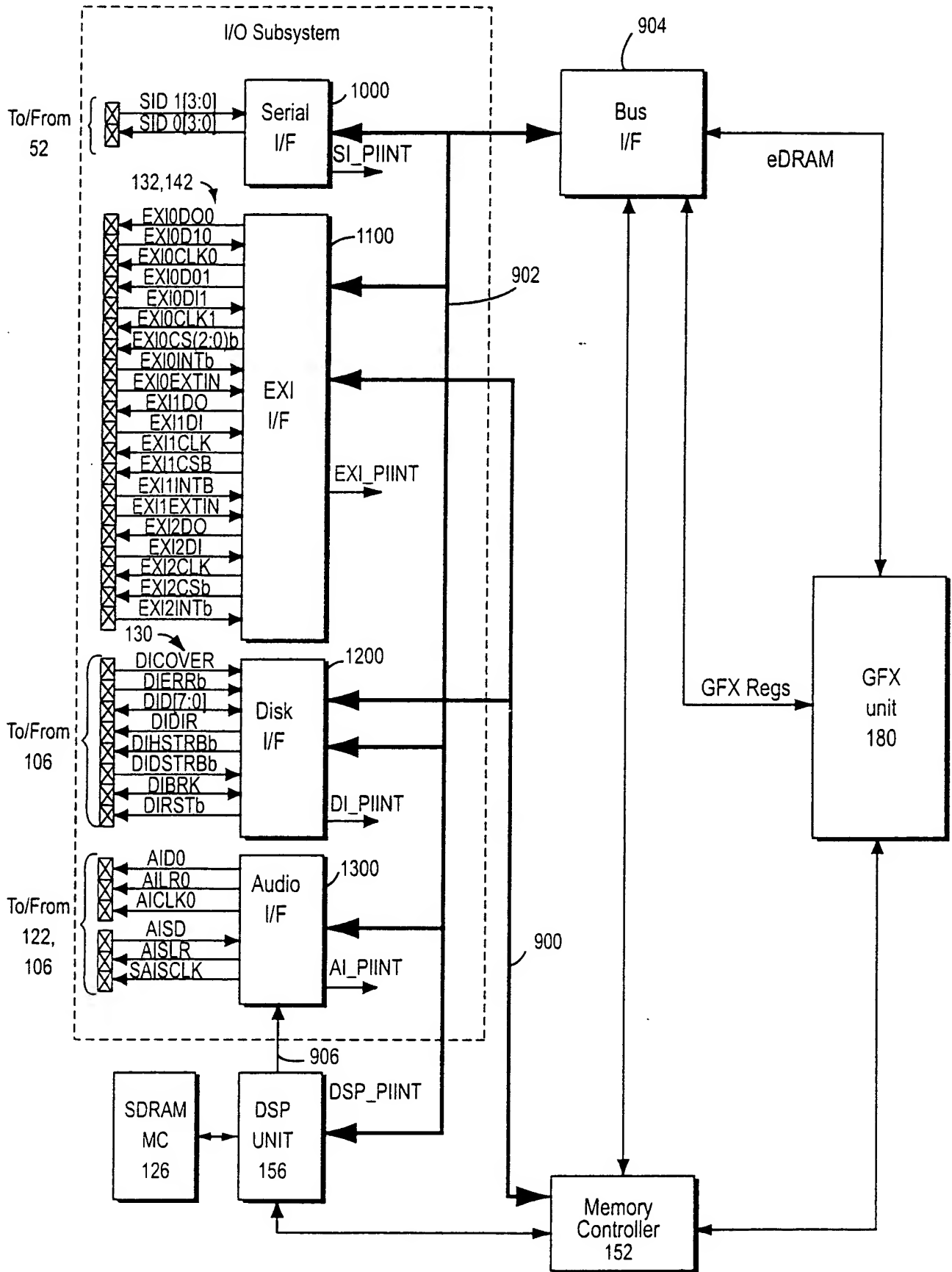


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

Fig. 6 EXAMPLE INPUT/OUTPUT SUBSYSTEM



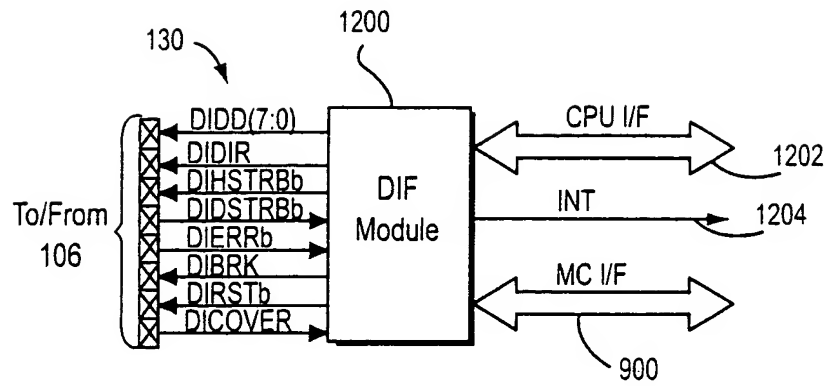


Fig. 7A
 EXAMPLE DISK INTERFACE

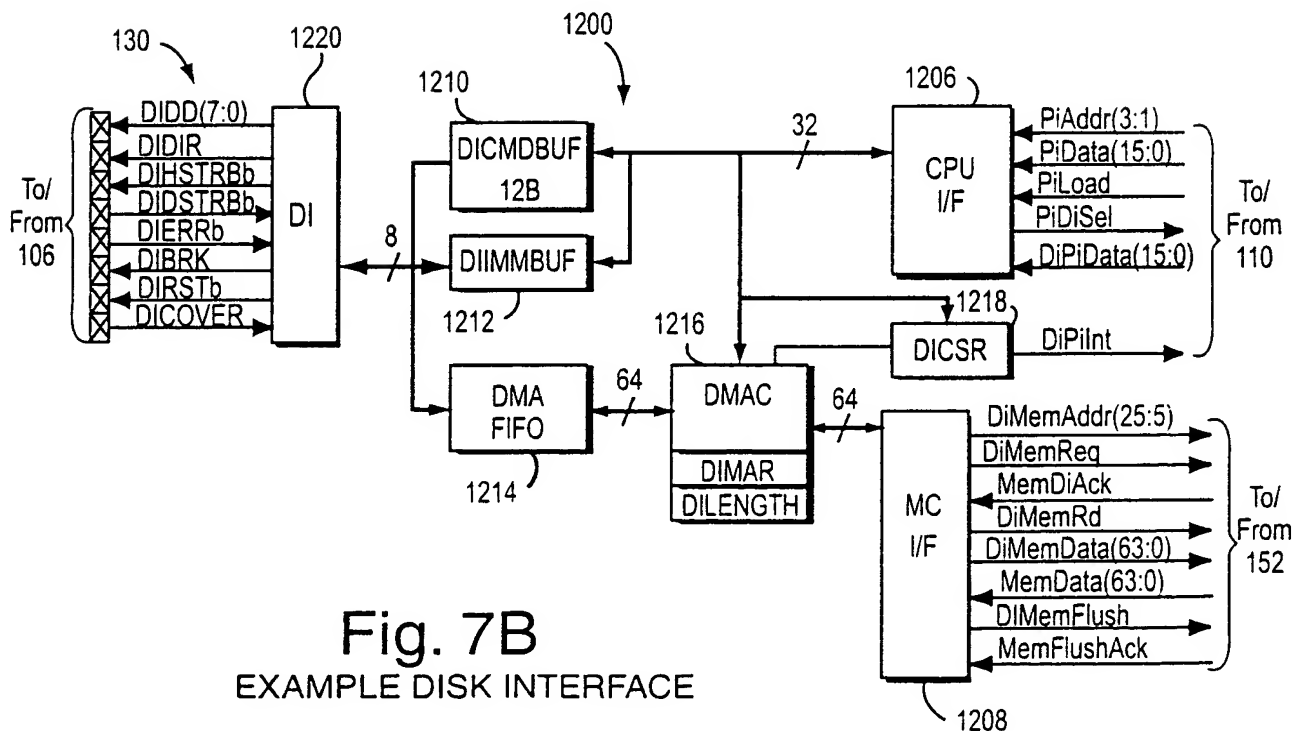


Fig. 7B
 EXAMPLE DISK INTERFACE

Register			Offset(hex)
31	16	15	0
DI Status Register (DISR)			0x00
DI Cover Register (DICCVR)			0x04
DI Command Buffer 0 (DICMDBUF0)			0x08
DI Command Buffer 1 (DICMDBUF1)			0x0C
DI Command Buffer 2 (DICMDBUF2)			0x10
DI Memory Address Register (DIMAR)			0x14
DI DMA Length Register (DILENGTH)			0x18
DI Control Register (DICR)			0x1C
DI Immediate Data Buffer (DIMMBUF)			0x20
DI Configuration Register (DICFG)			0x24

Fig. 7C
 EXAMPLE DISK INTERFACE REGISTERS

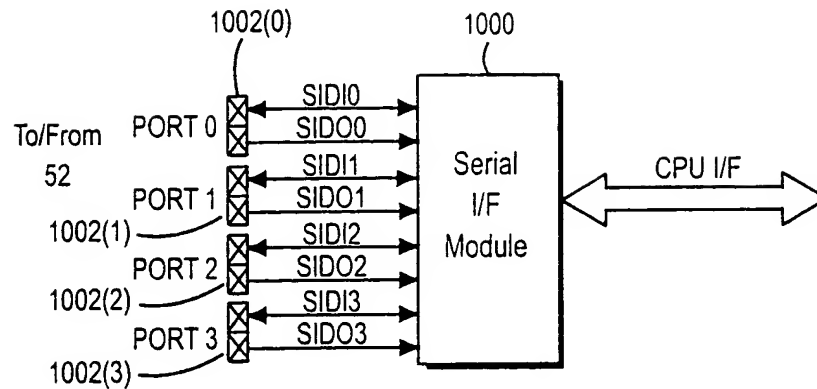


Fig. 8A
 EXAMPLE SERIAL INTERFACE

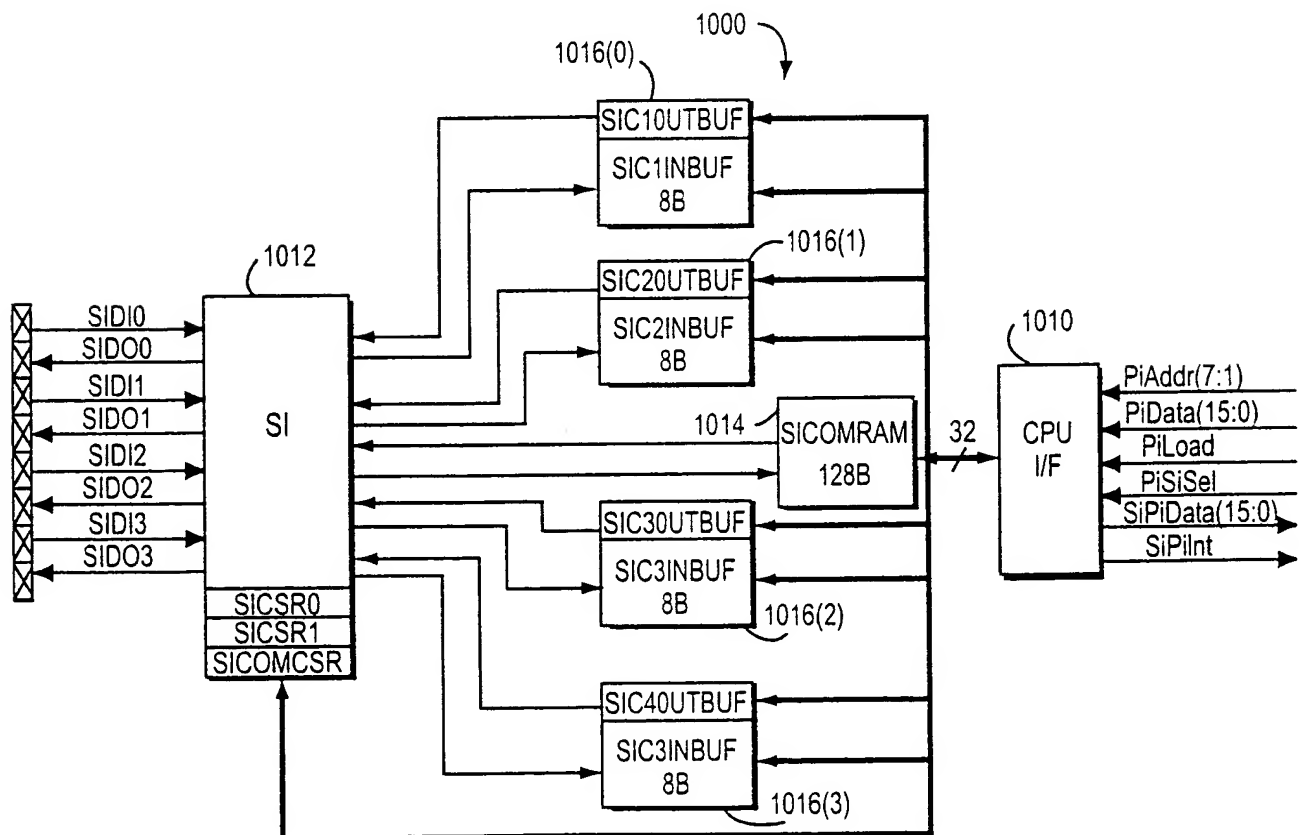


Fig. 8B
 EXAMPLE SERIAL INTERFACE

Register			Offset(hex)
31	16	15	0
SI Channel 0 Output Buffer (SIC0OUTBUF)			0x00
SI Channel 0 Output Buffer H(SIC0INBUFH)			0x04
SI Channel 0 Output Buffer L(SIC0INBUFL)			0x08
SI Channel 1 Output Buffer (SIC1OUTBUF)			0x0C
SI Channel 1 Input Buffer H(SIC1INBUFH)			0x10
SI Channel 1 Input Buffer L(SIC1INBUFL)			0x14
SI Channel 2 Output Buffer (SIC2OUTBUF)			0x18
SI Channel 2 Input Buffer H(SIC2INBUFH)			0x1C
SI Channel 2 Input Buffer L(SIC2INBUFL)			0x20
SI Channel 3 Output Buffer (SIC3OUTBUF)			0x24
SI Channel 3 Input Buffer H(SIC3INBUFH)			0x28
SI Channel 3 Input Buffer L(SIC3INBUFL)			0x2C
SI Poll Control Register (SIPOLL)			0x30
SI Communication Control Status Register (SICOMCSR)			0x34
SI Status Register (SISR)			0x38
SI EXI Lock Register (SIEXILK)			0x3C
SI Communication RAM (128 Bytes)			0x80-0xFF

Fig. 8C
 EXAMPLE SERIAL INTERFACE REGISTERS

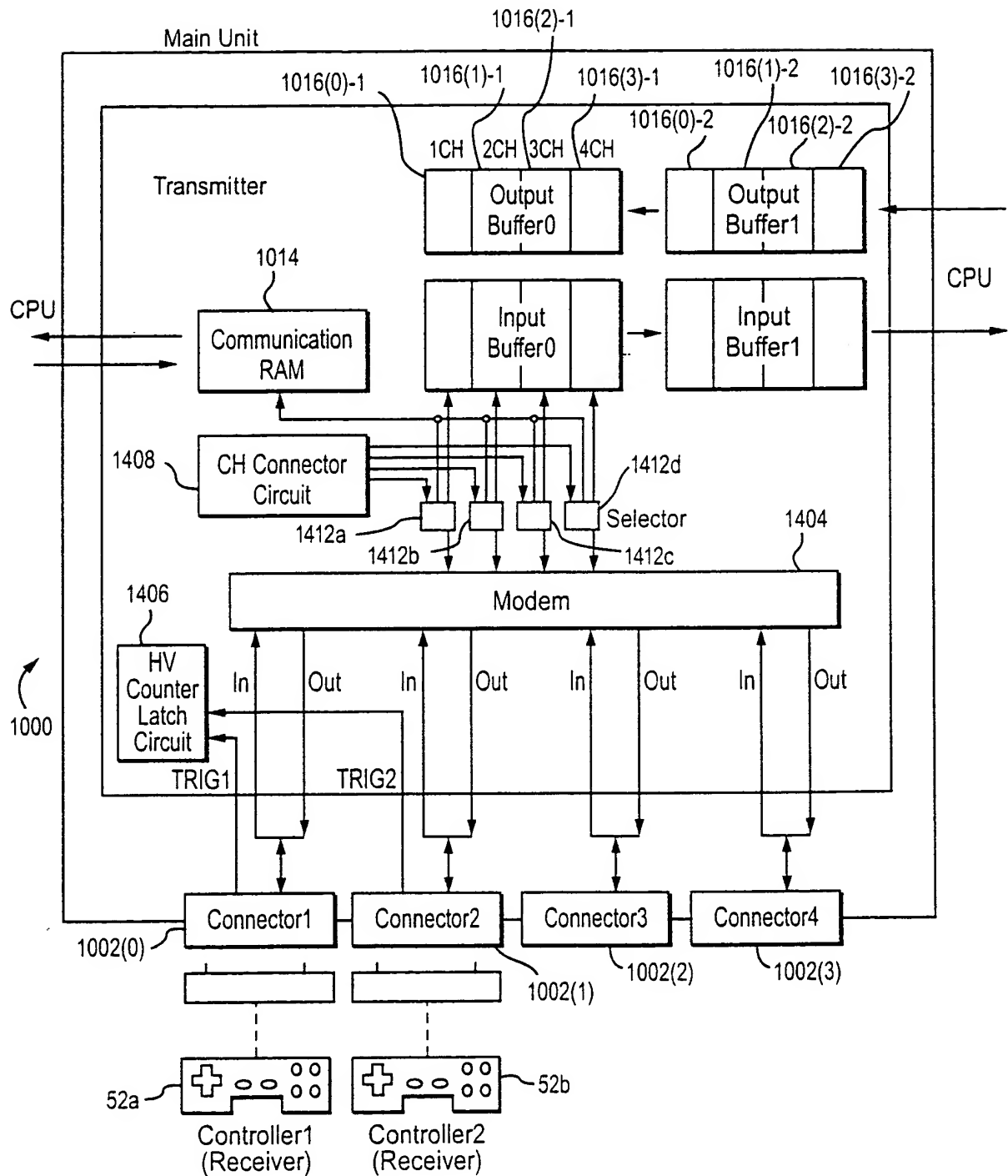


Fig. 8D
 EXAMPLE SERIAL INTERFACE

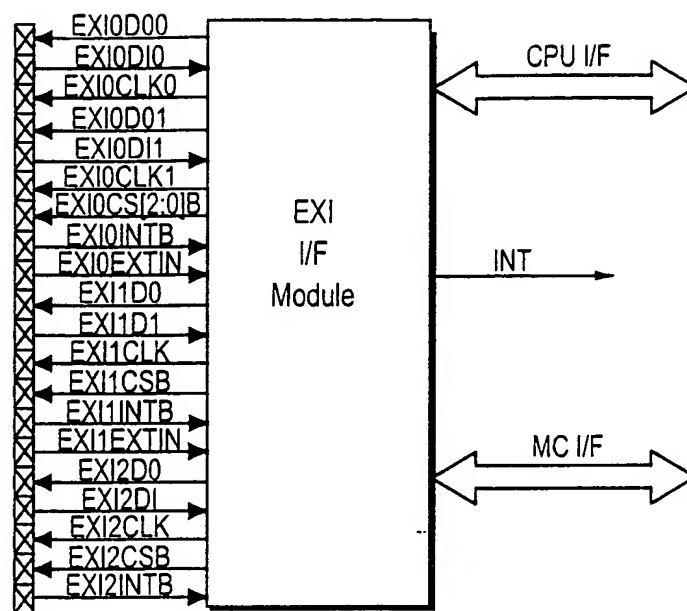


Fig. 9A
 EXAMPLE EXTERNAL INTERFACE

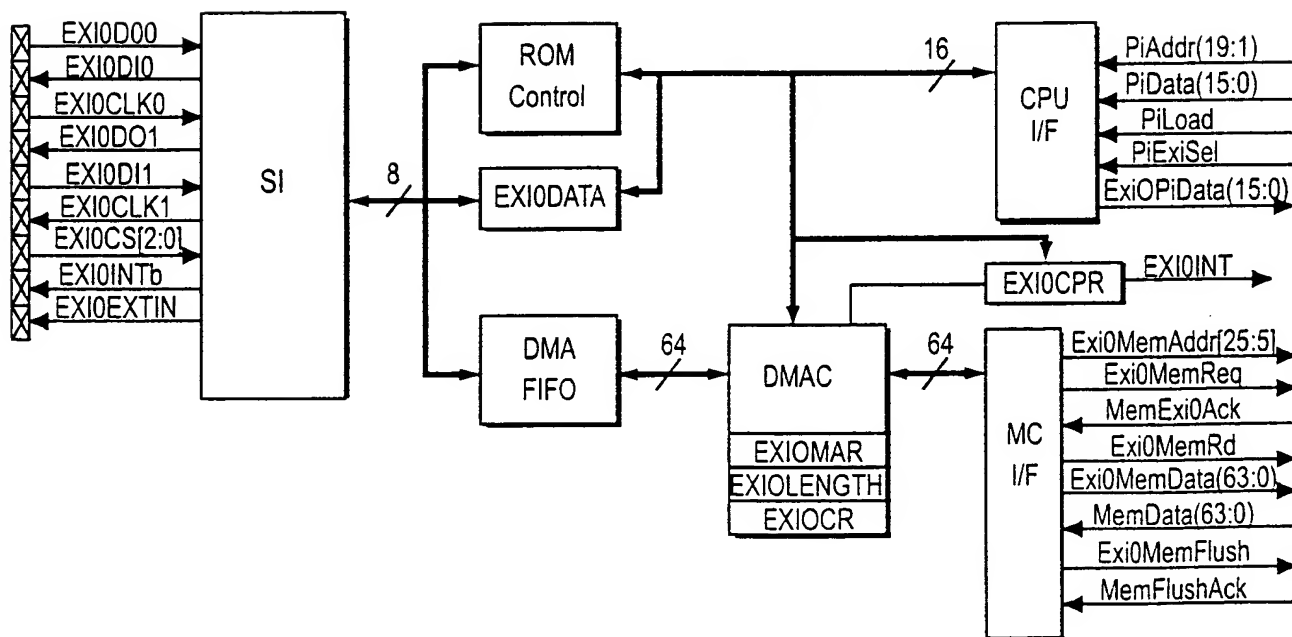


Fig. 9B
 EXAMPLE EXTERNAL CHANNEL 0 INTERFACE

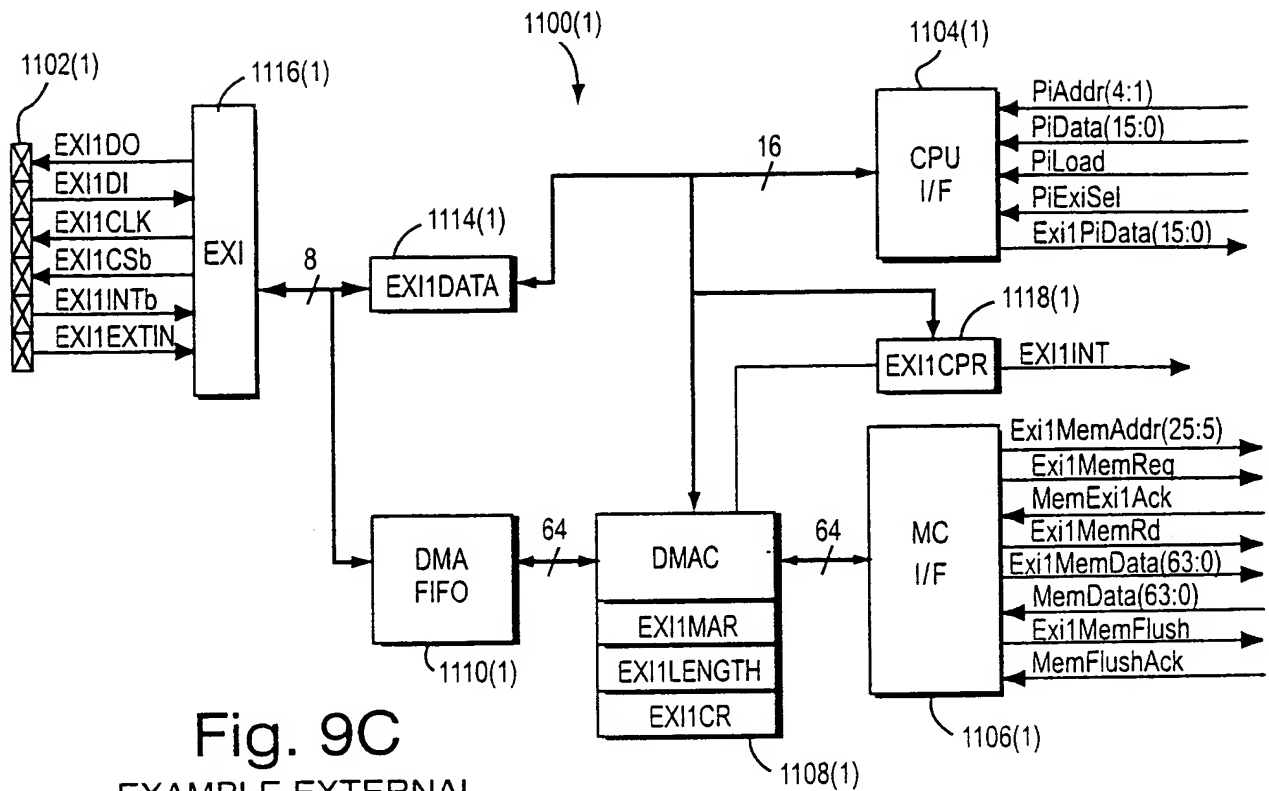


Fig. 9C
 EXAMPLE EXTERNAL
 CHANNEL 1 INTERFACE

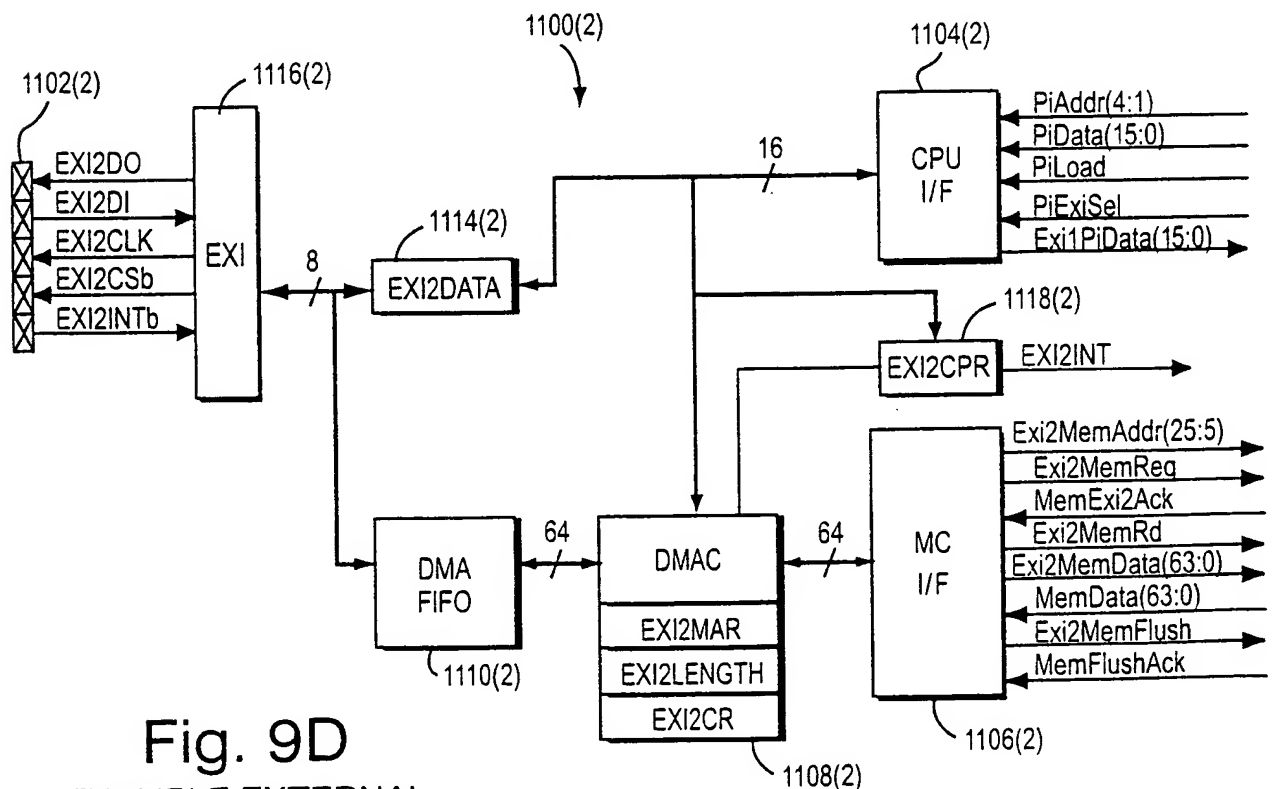


Fig. 9D
 EXAMPLE EXTERNAL
 CHANNEL 2 INTERFACE

Register				Offset(hex)
31	16	15	0	
EXI0 Channel Parameter Register (EXI0CPR)				0x00
EXI0 Memory Address Register (EXI0MAR)				0x04
EXI0 DMA Length (EXI0LENGTH)				0x08
EXI0 Control Register (EXI0CR)				0x0C
EXI0 Data Register (EXI0DATA)				0x10
EXI1 Channel Parameter Register (EXI1CPR)				0x14
EXI1 Memory Address Register (EXI1MAR)				0x18
EXI1 DMA Length (EXI1LENGTH)				0x1C
EXI1 Control Register (EXI1CR)				0x20
EXI1 Data Register (EXI1DATA)				0x24
EXI2 Channel Parameter Register (EXI2CPR)				0x28
EXI2 Memory Address Register (EXI2MAR)				0x2C
EXI2 DMA Length (EXI2LENGTH)				0x30
EXI2 Control Register (EXI2CR)				0x34
EXI2 Data Register (EXI2DATA)				0x38
ROM Area (1MB)				0xFFF00000

Fig. 9E
EXAMPLE EXTERNAL INTERFACE REGISTERS

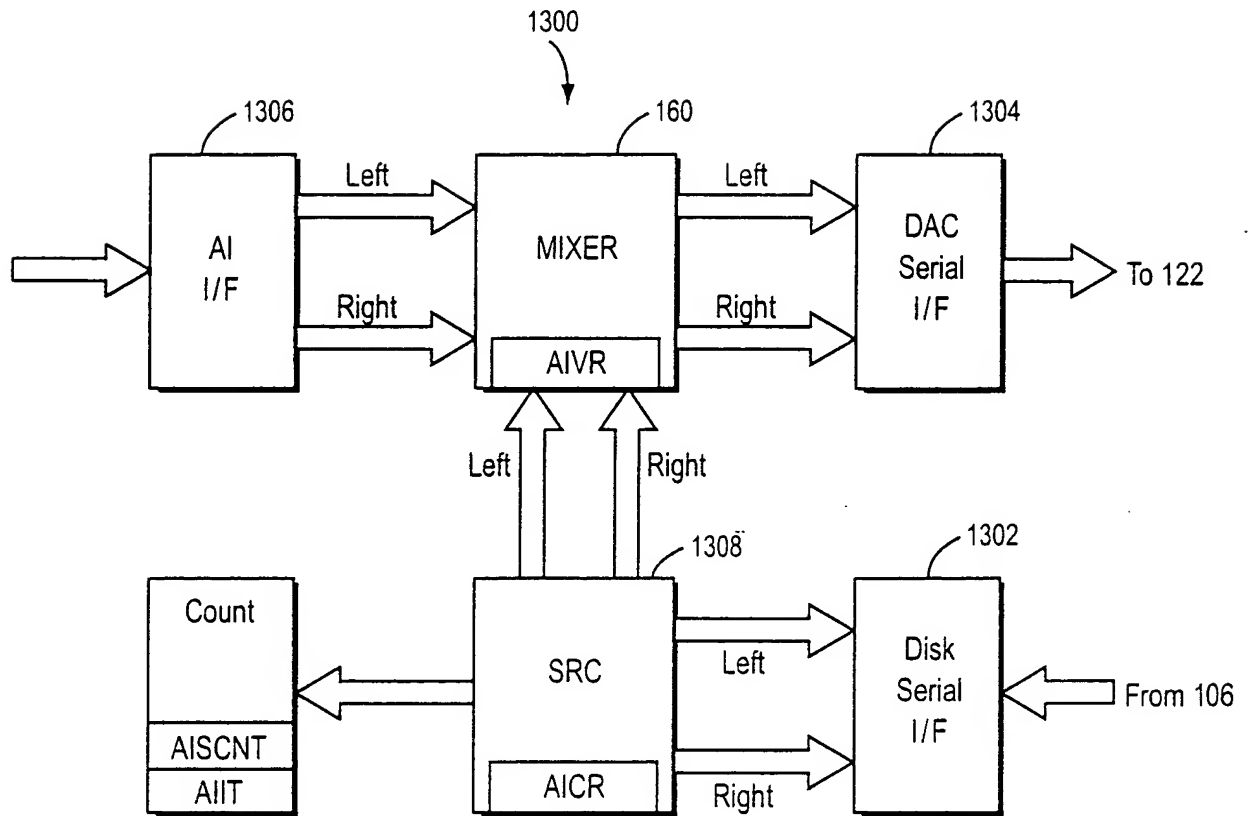


Fig. 10A
 EXAMPLE AUDIO INTERFACES

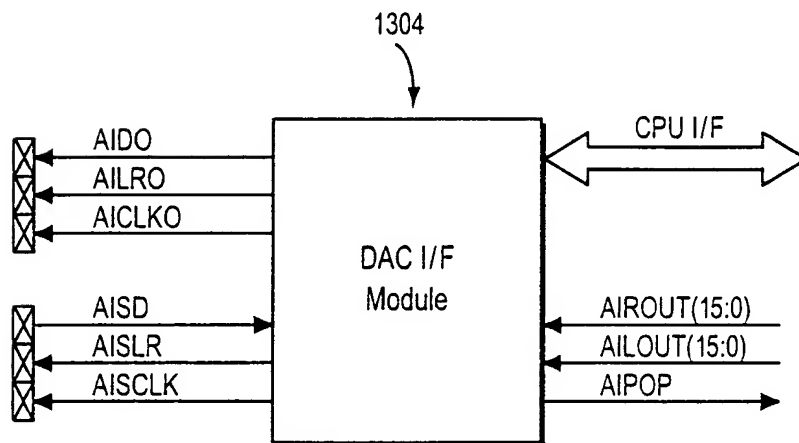


Fig. 10B
 EXAMPLE AUDIO DAC INTERFACES

Register				Offset(hex)
31	16	15	0	
AI Control Register (AICR)				0x00
AI Volume Register (AIVR)				0x04
AI Sample Count Register (AISCNT)				0x08
AI Interrupt Timing Register (AIIT)				0x0C

Fig. 10C
EXAMPLE AUDIO INTERFACES REGISTERS

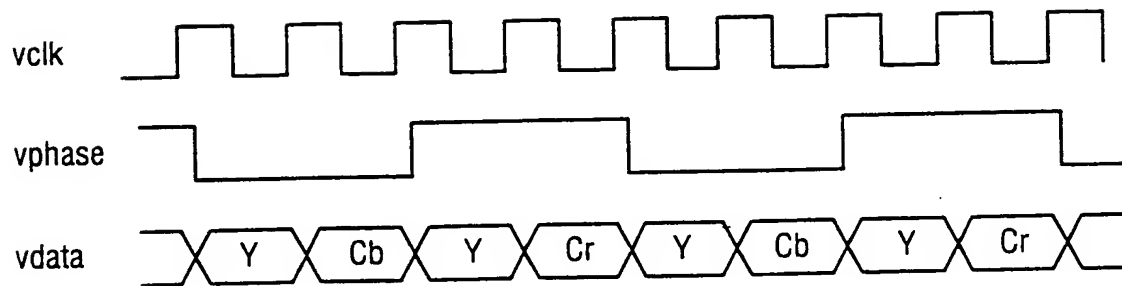


Fig. 11A

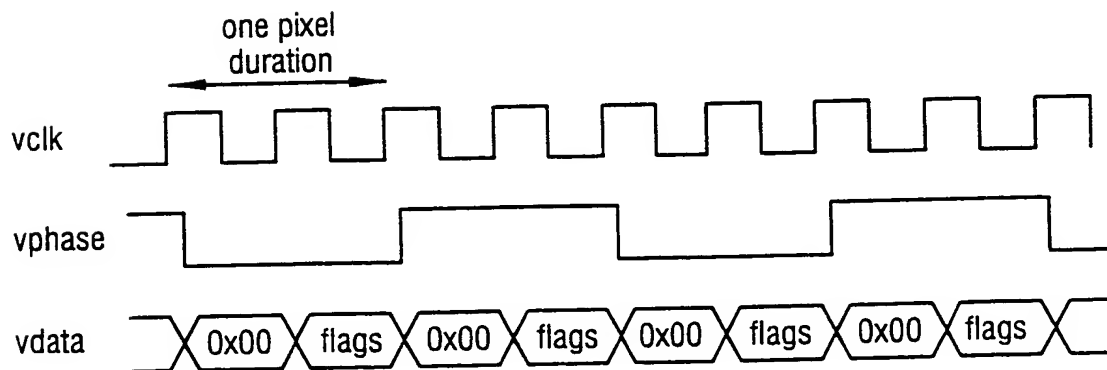


Fig. 11B

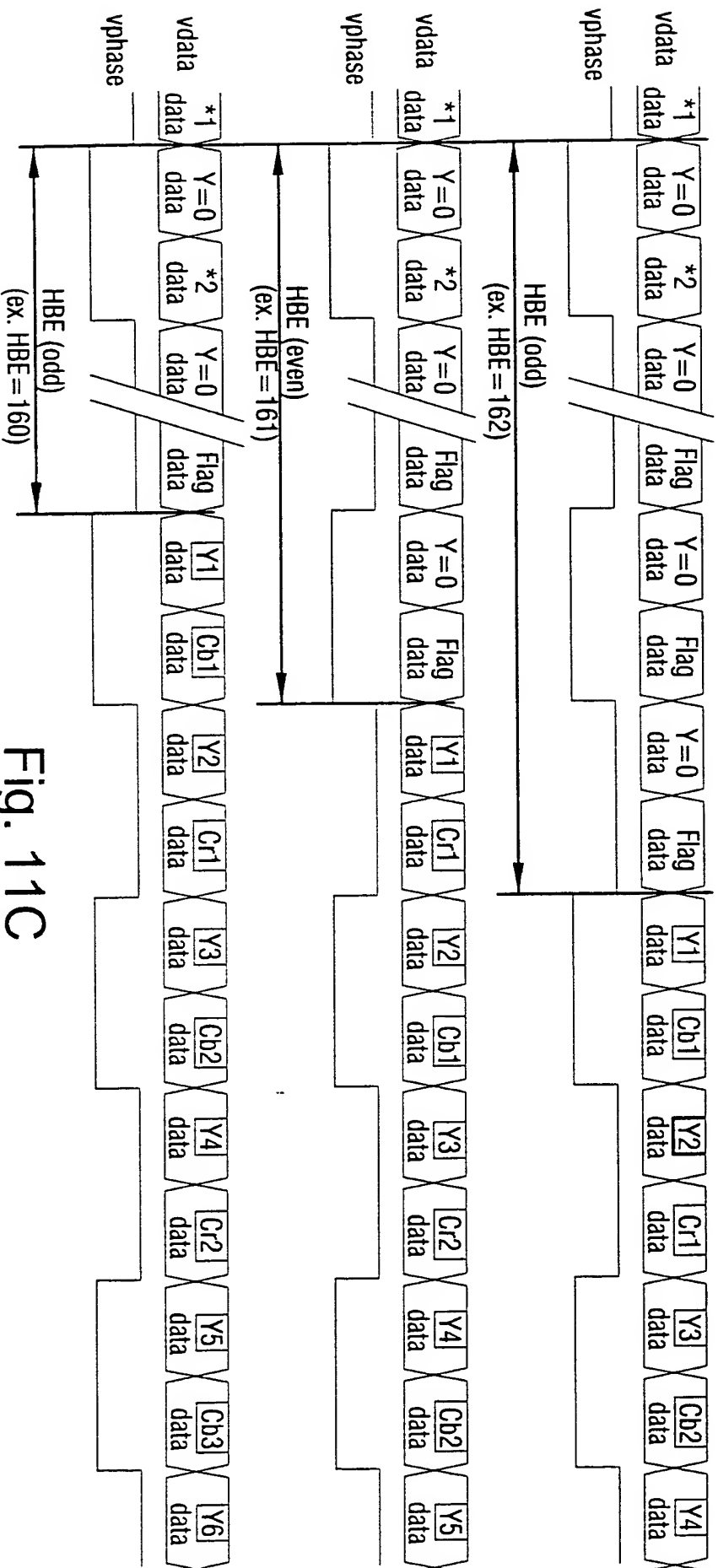


Fig. 11C

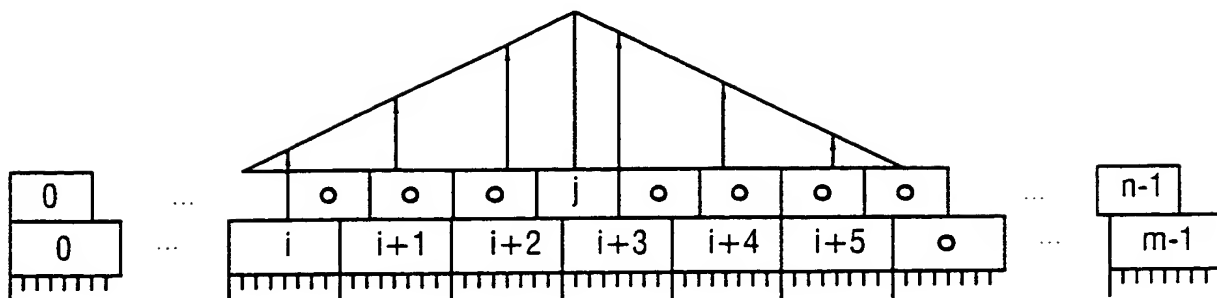


Fig. 11D

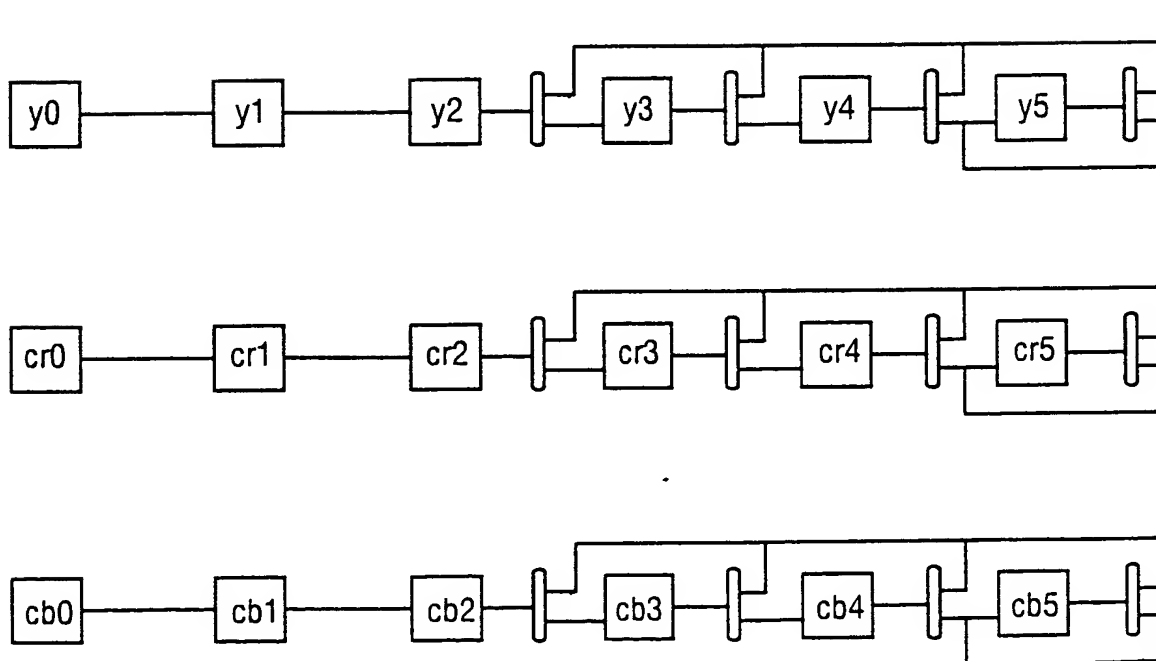


Fig. 11E

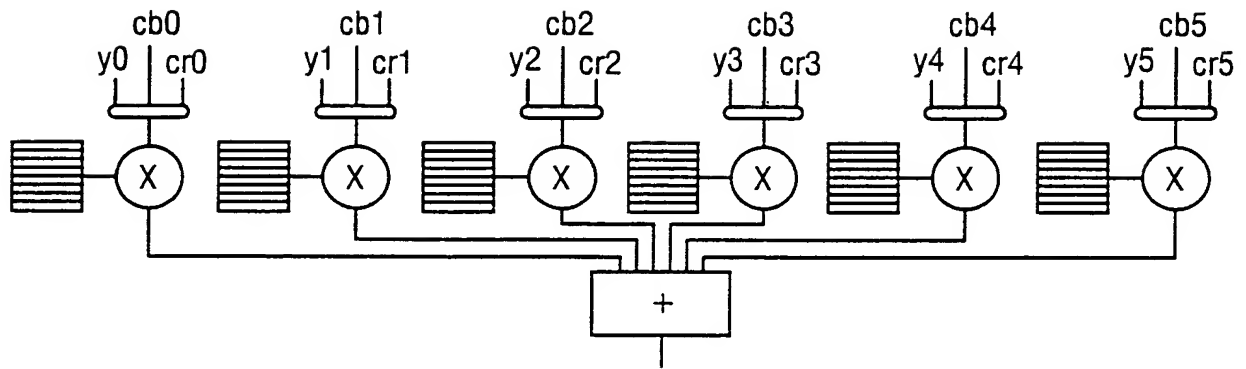


Fig. 11F

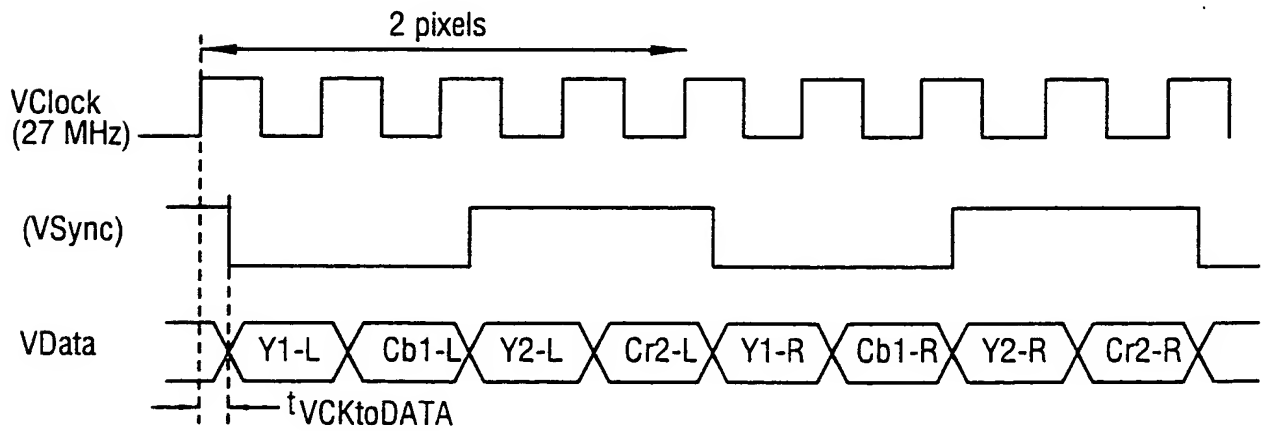


Fig. 11G

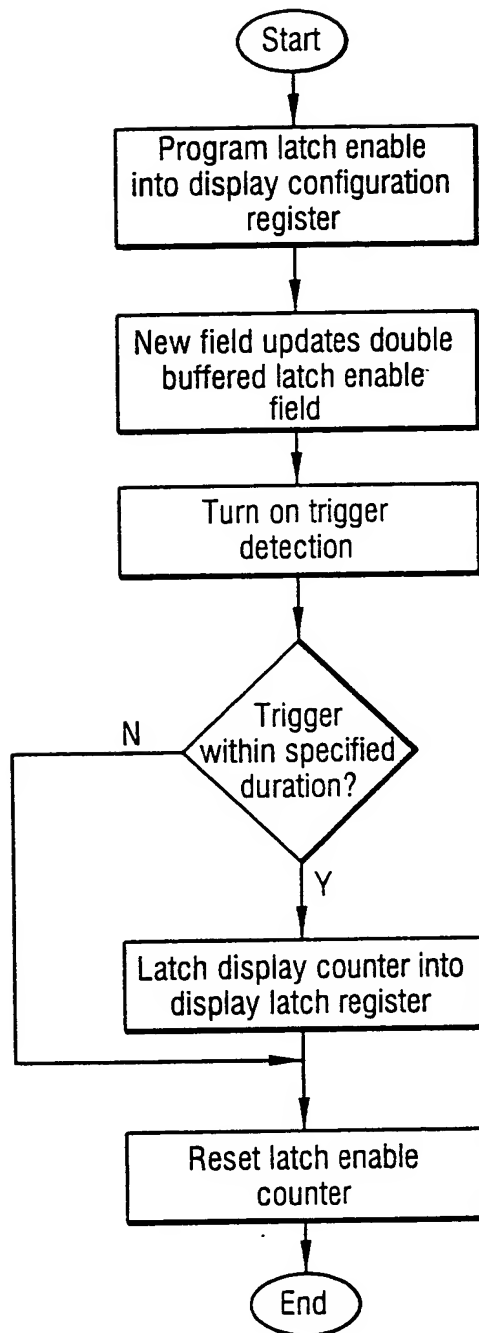


Fig. 11H

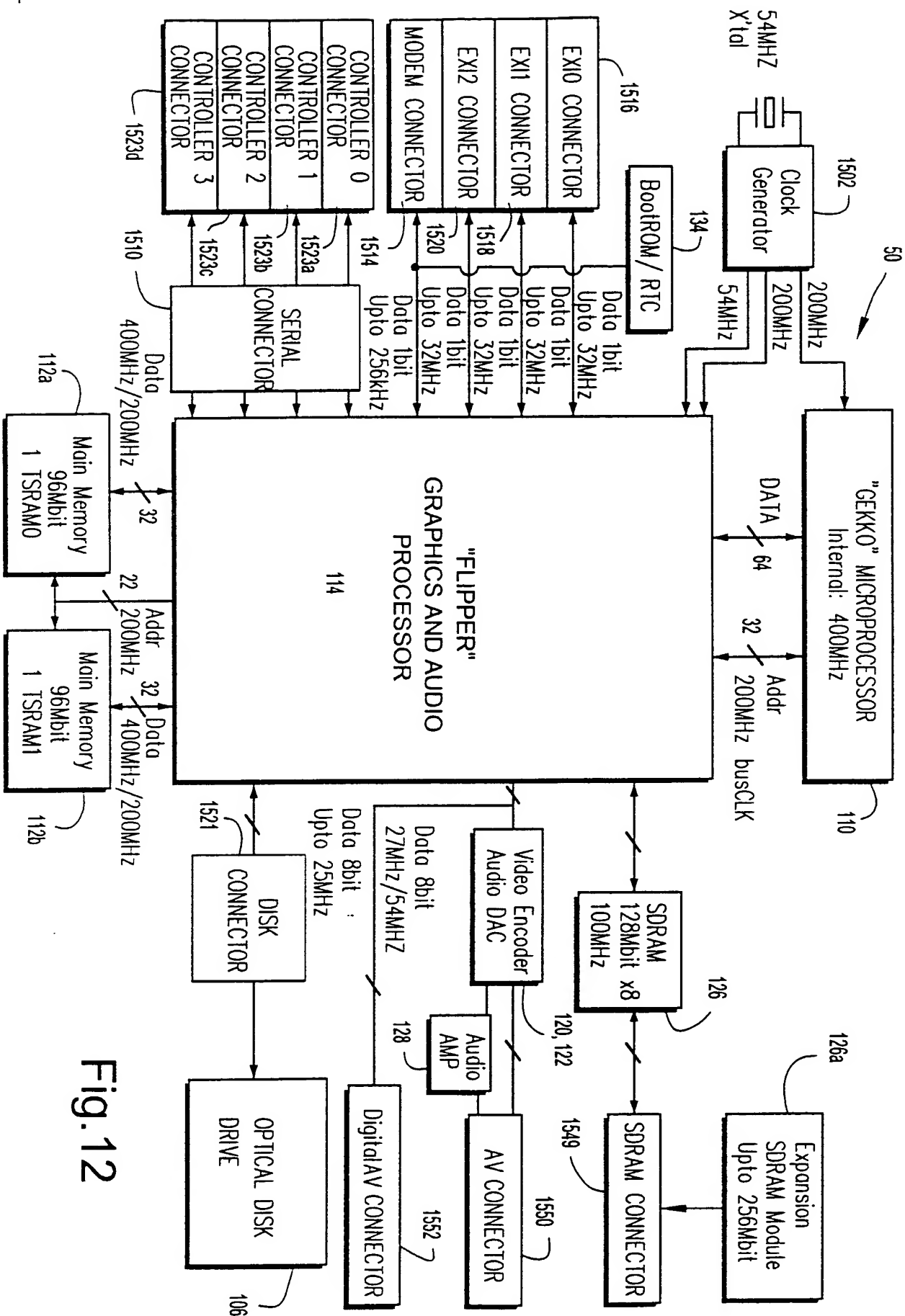


Fig.12

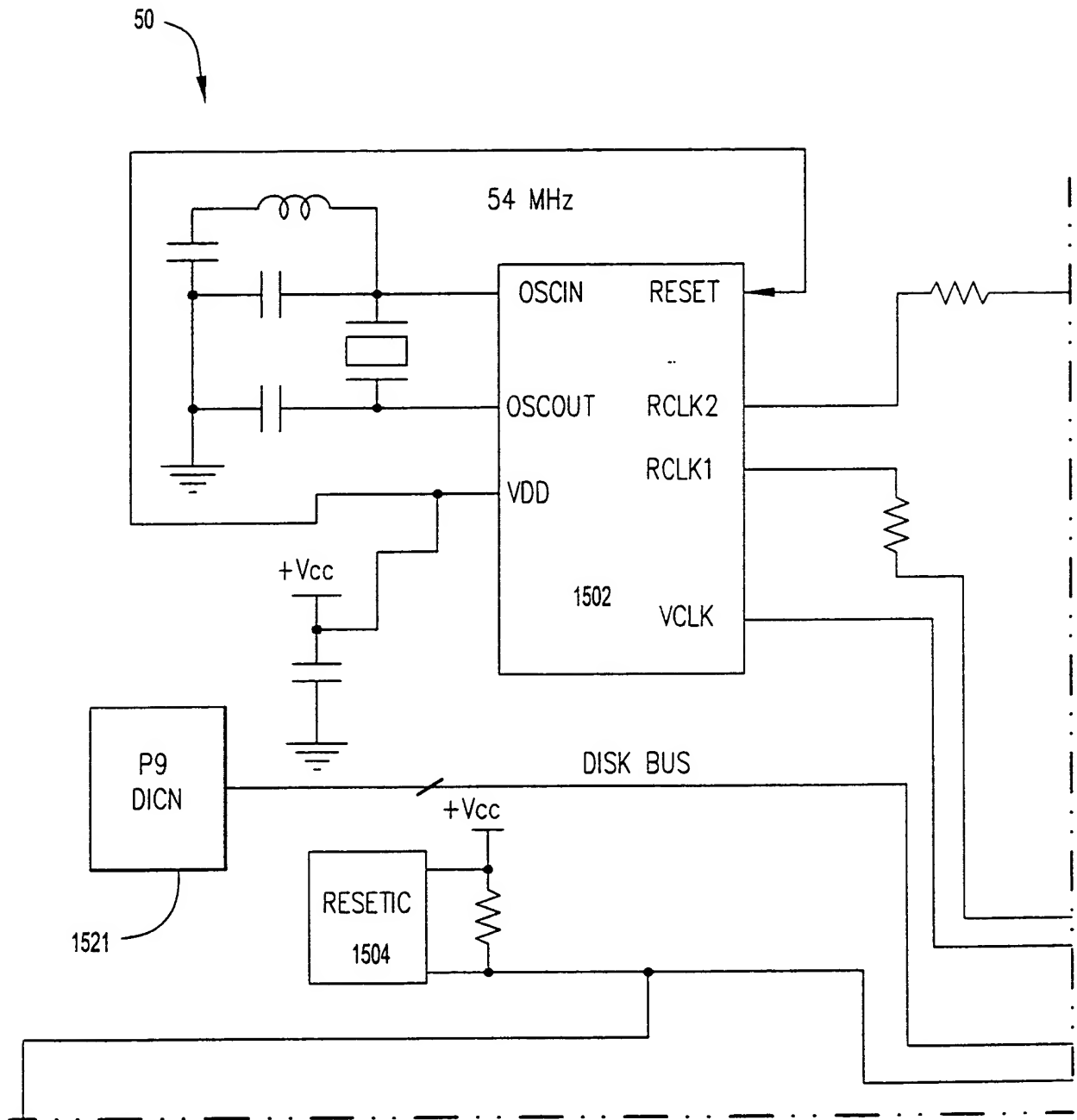
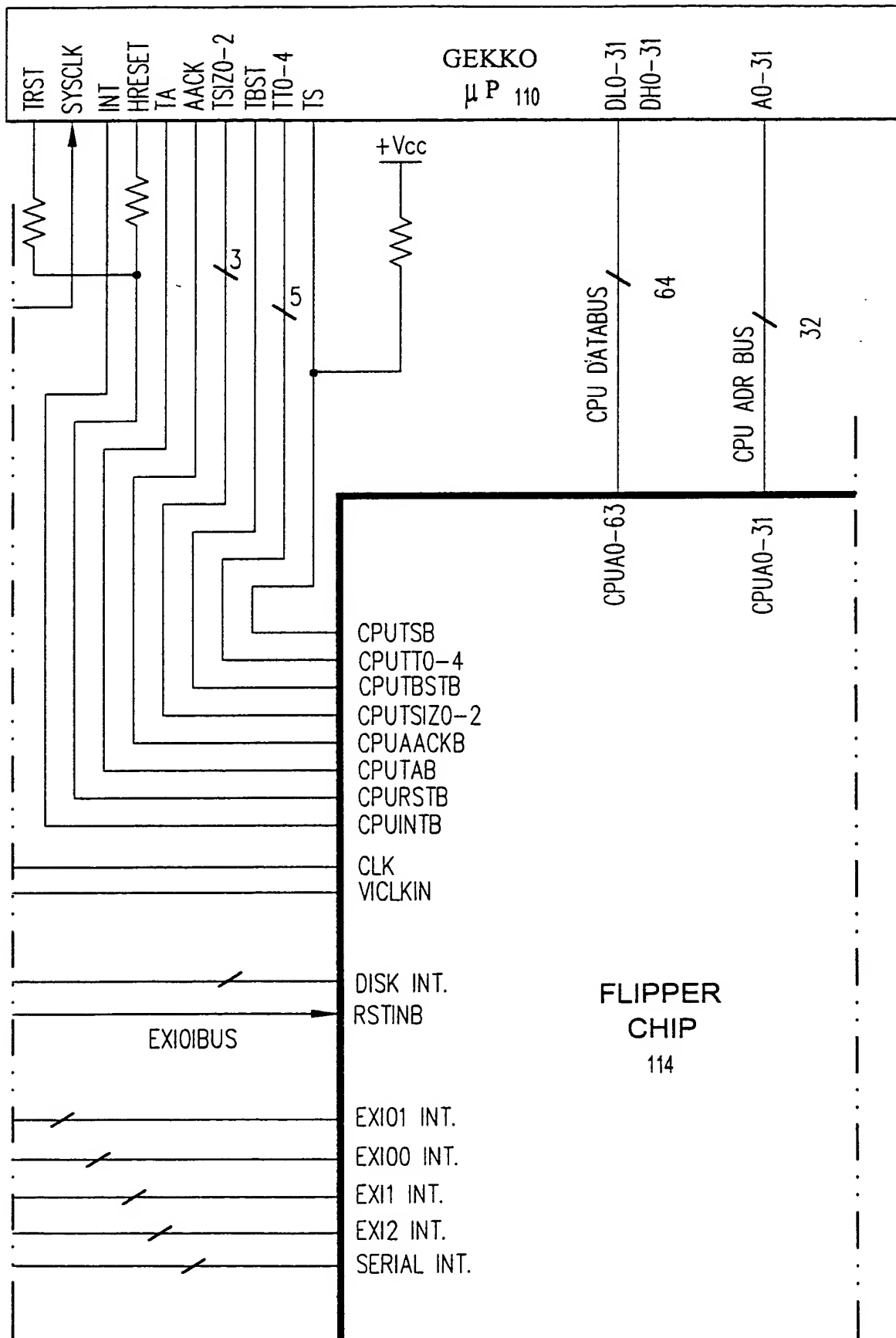
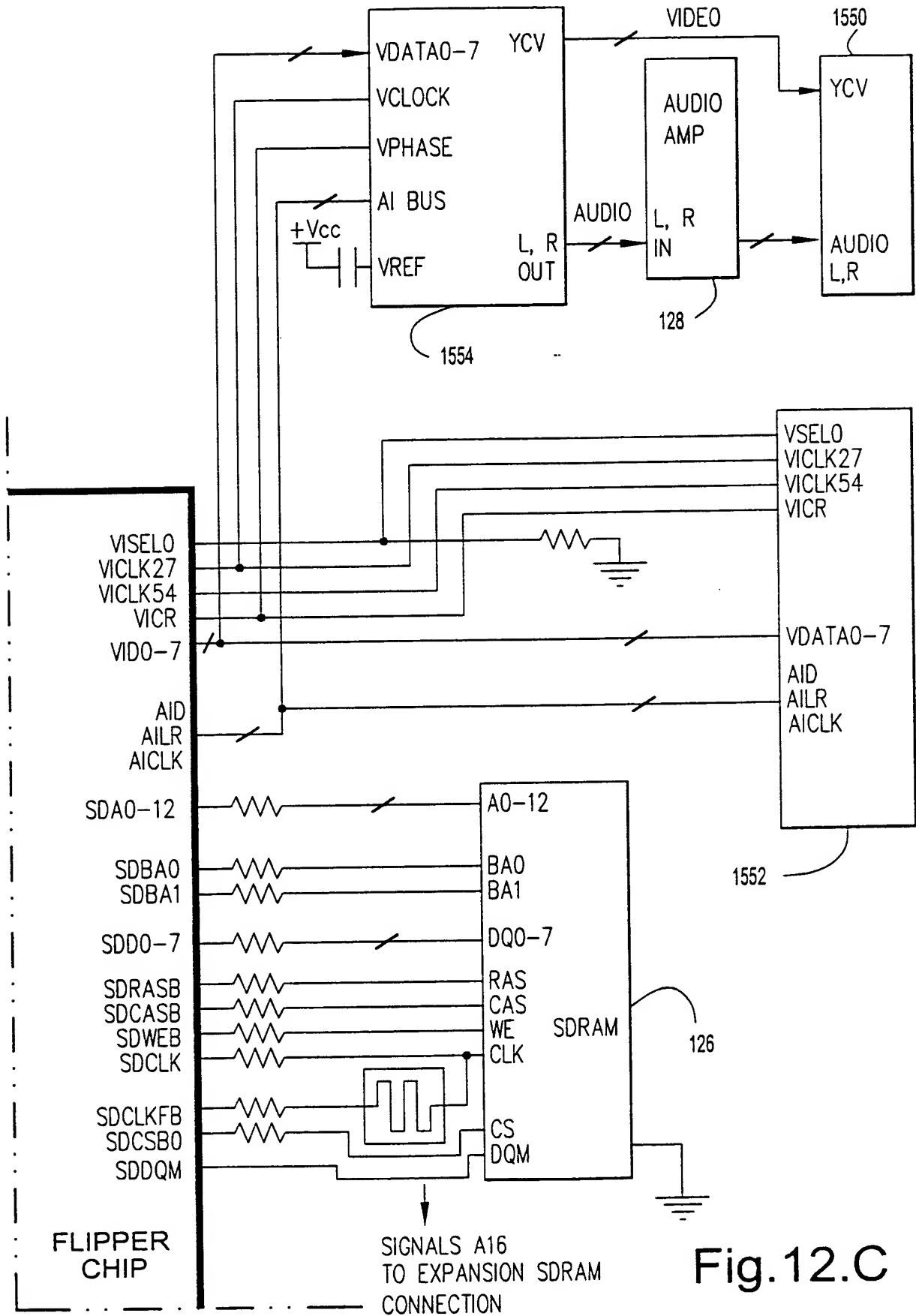


Fig.12A

Fig.12B





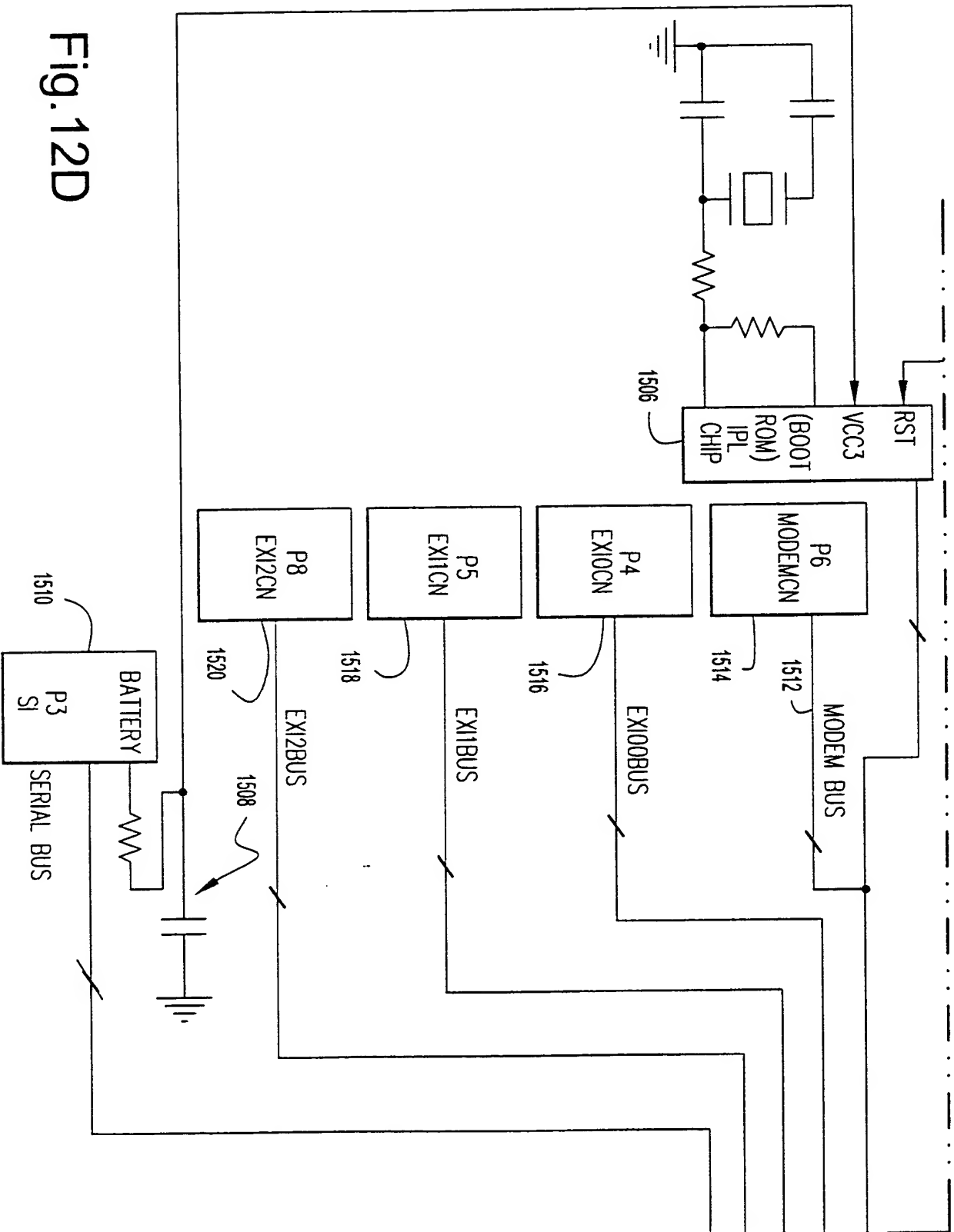


Fig. 12D

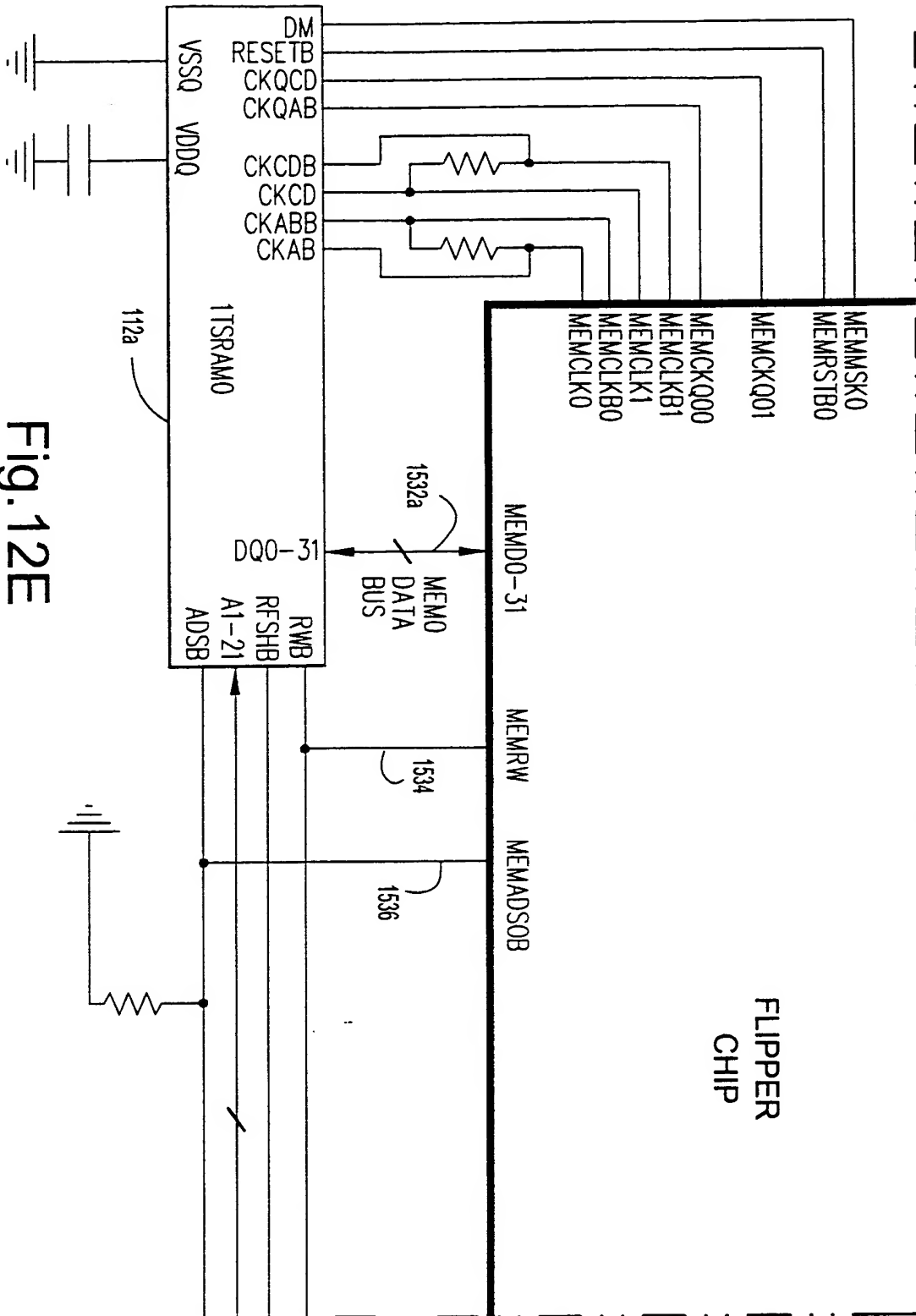


Fig. 12E

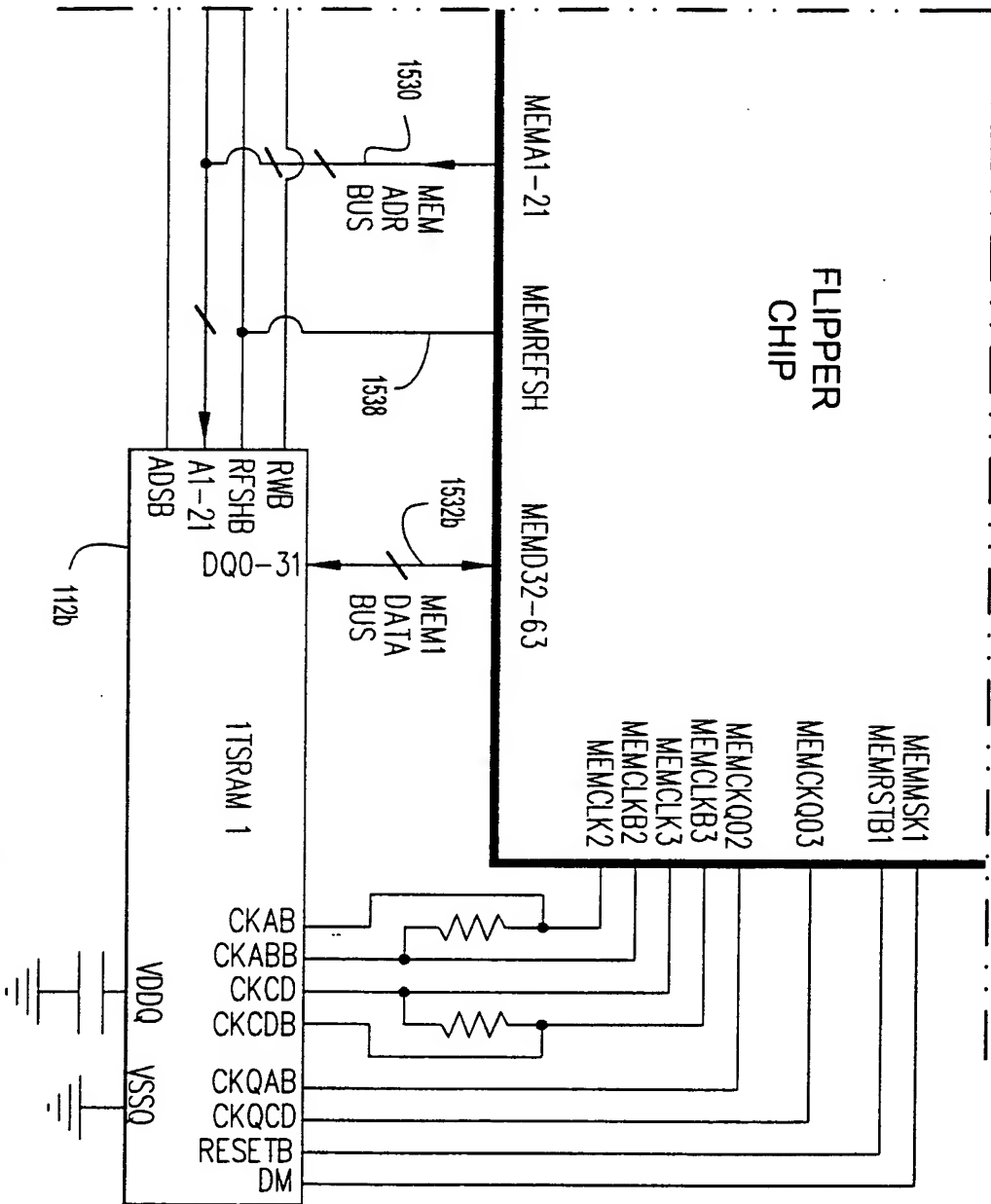


Fig. 12F

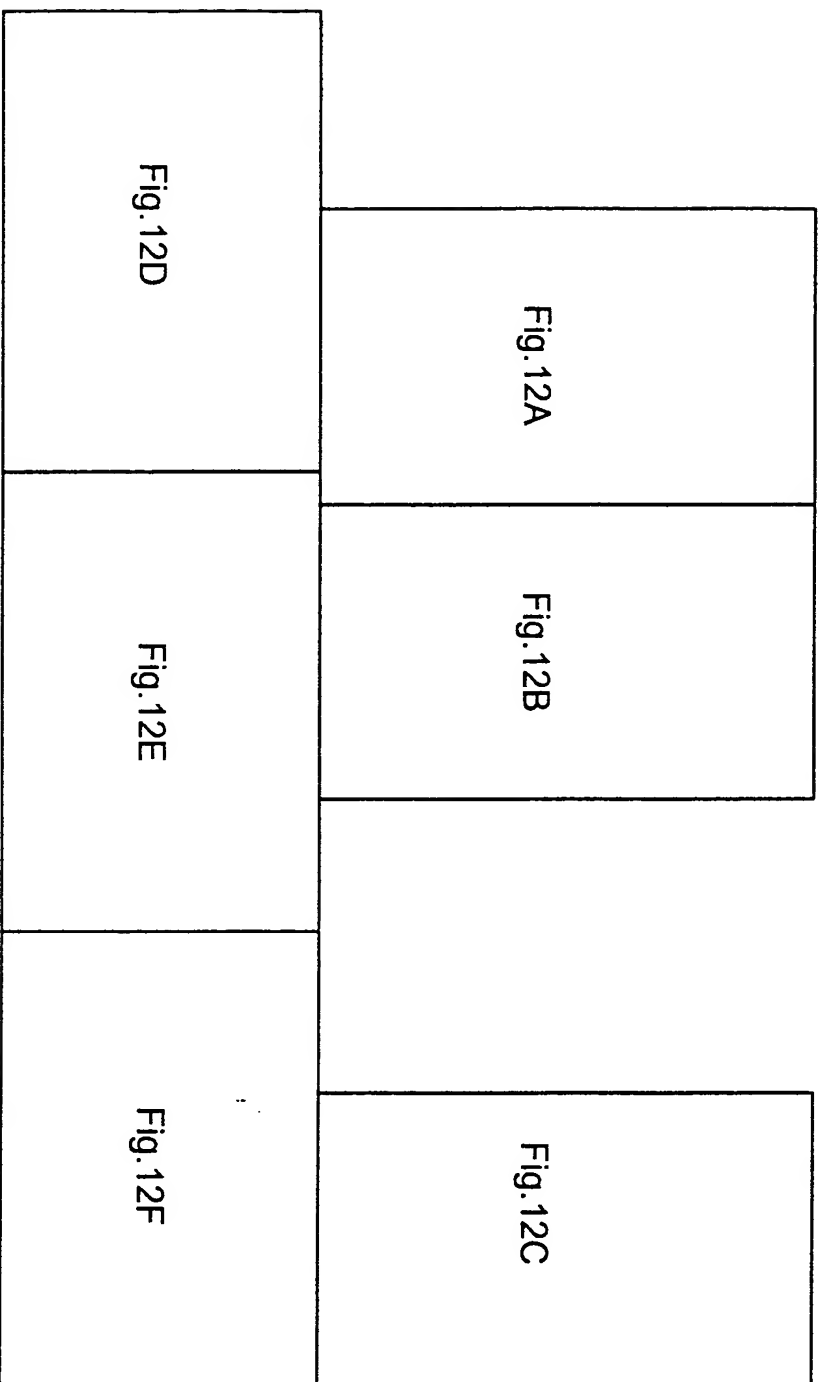


Fig. 12G

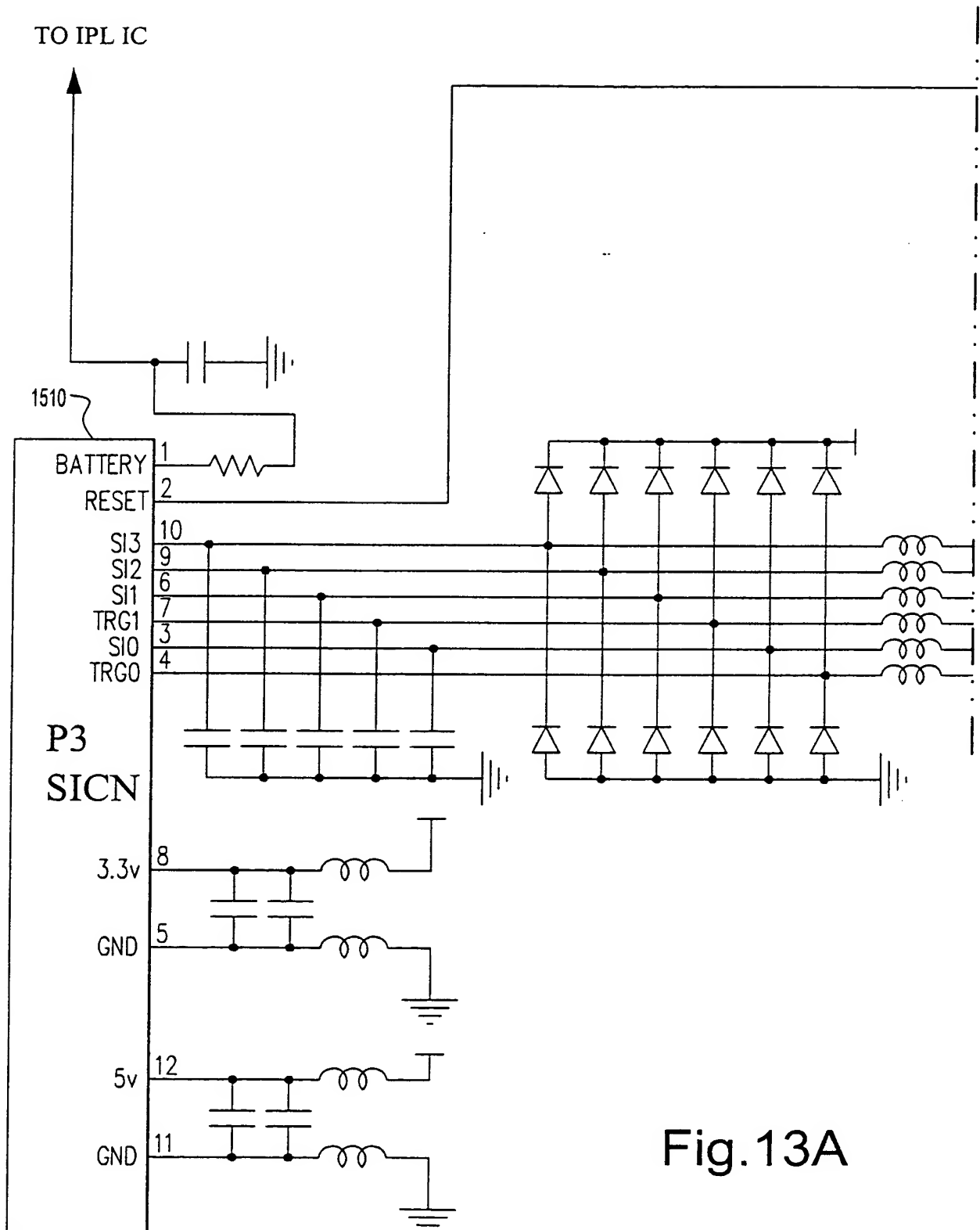


Fig.13A

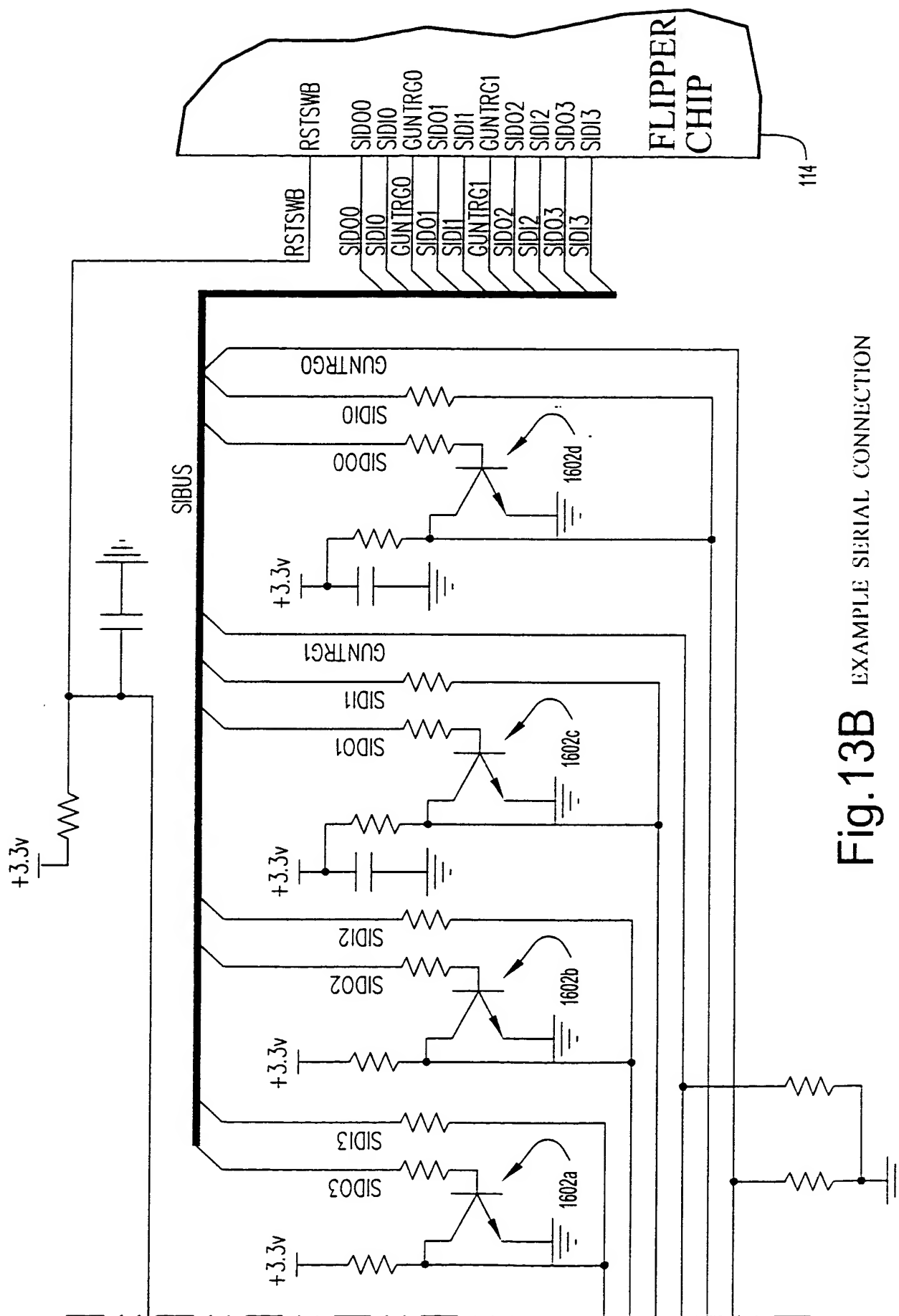


Fig. 13B EXAMPLE SERIAL CONNECTION

Fig. 14

EXAMPLE CONTROLLER PORT CONNECTION

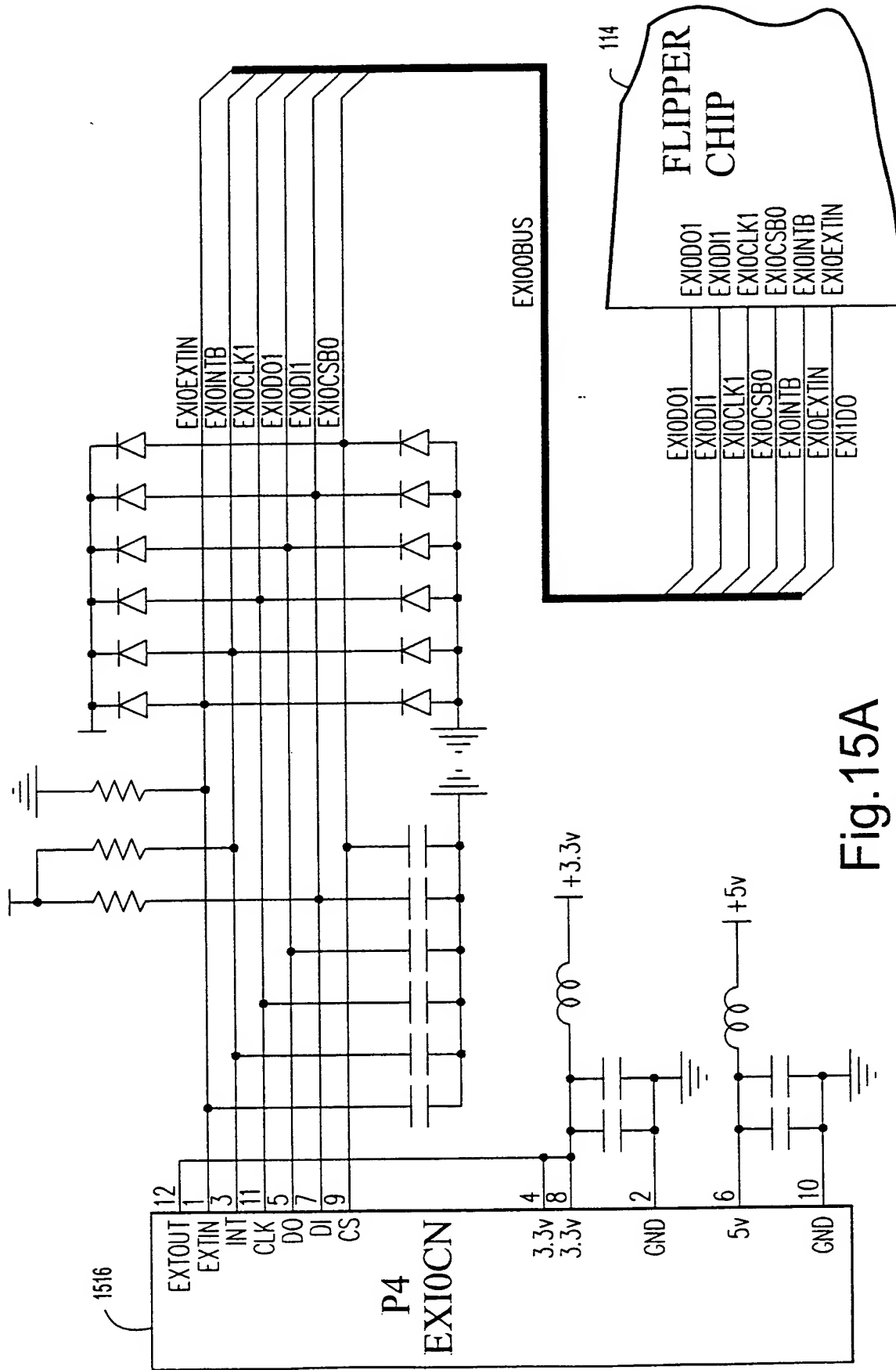


Fig. 15A

EXAMPLE EXTERNAL INTERFACE 0 CONNECTION

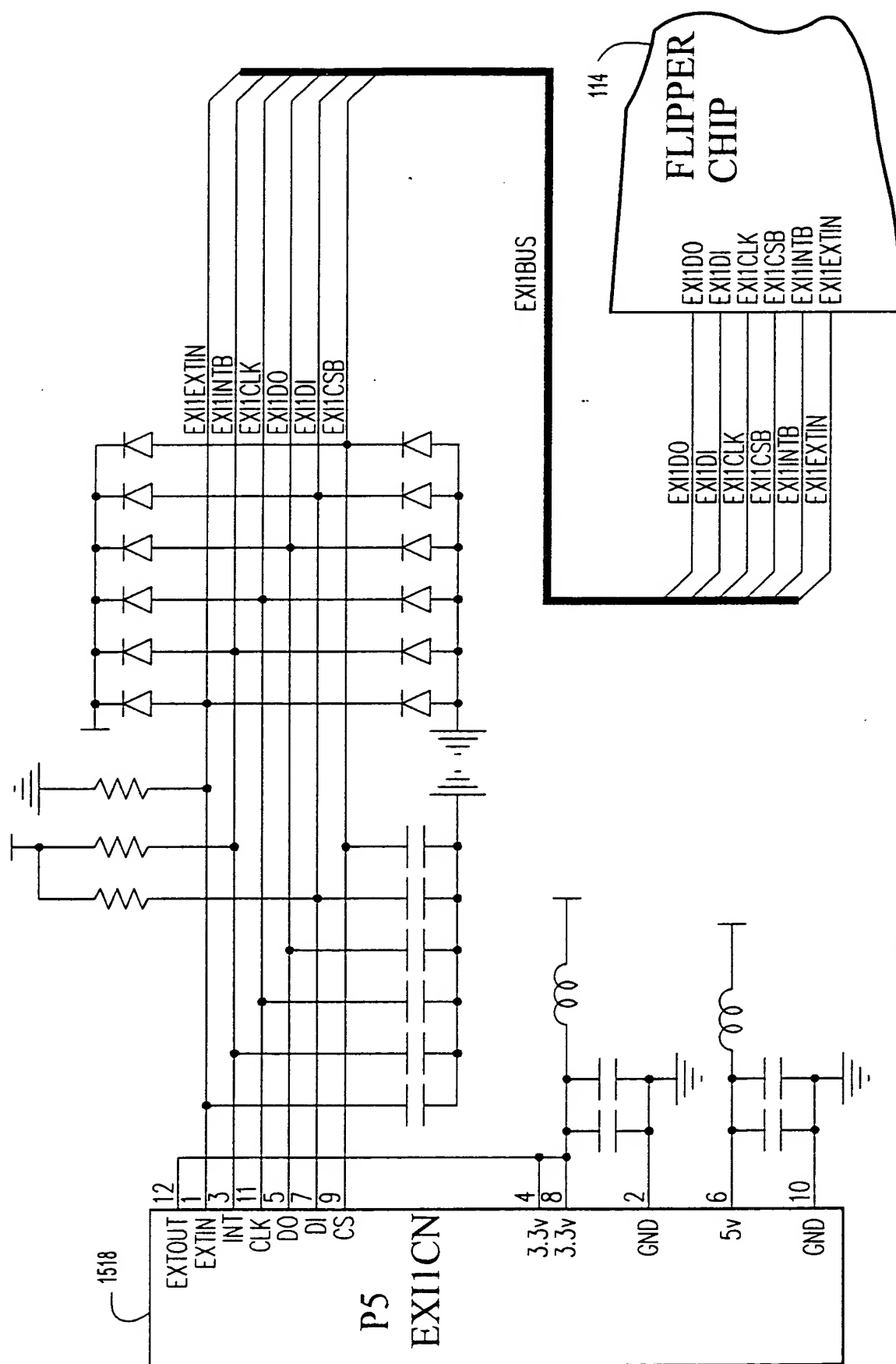


Fig.15B EXAMPLE EXTERNAL INTERFACE 1 CONNECTION

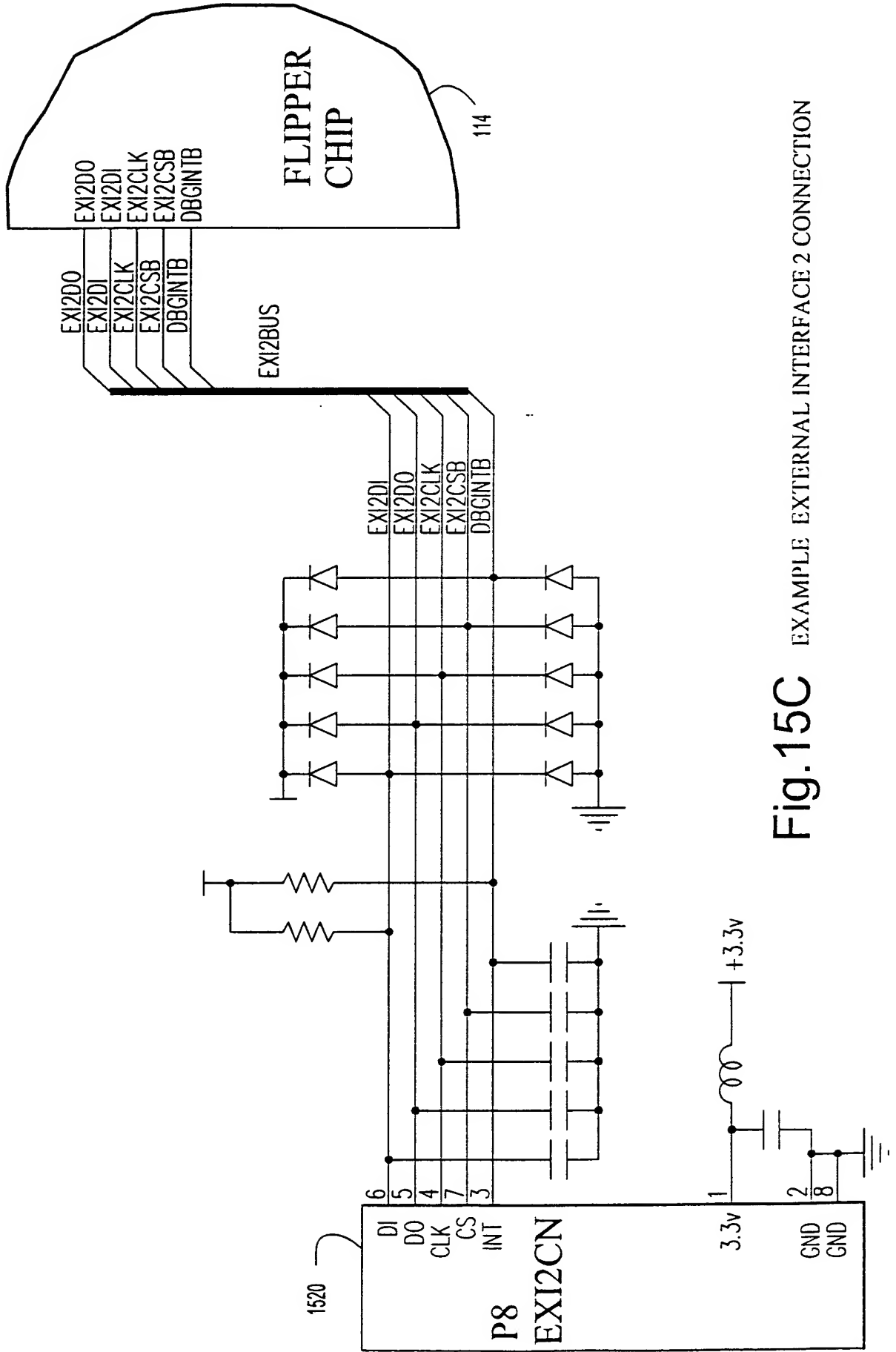


Fig.15C EXAMPLE EXTERNAL INTERFACE 2 CONNECTION

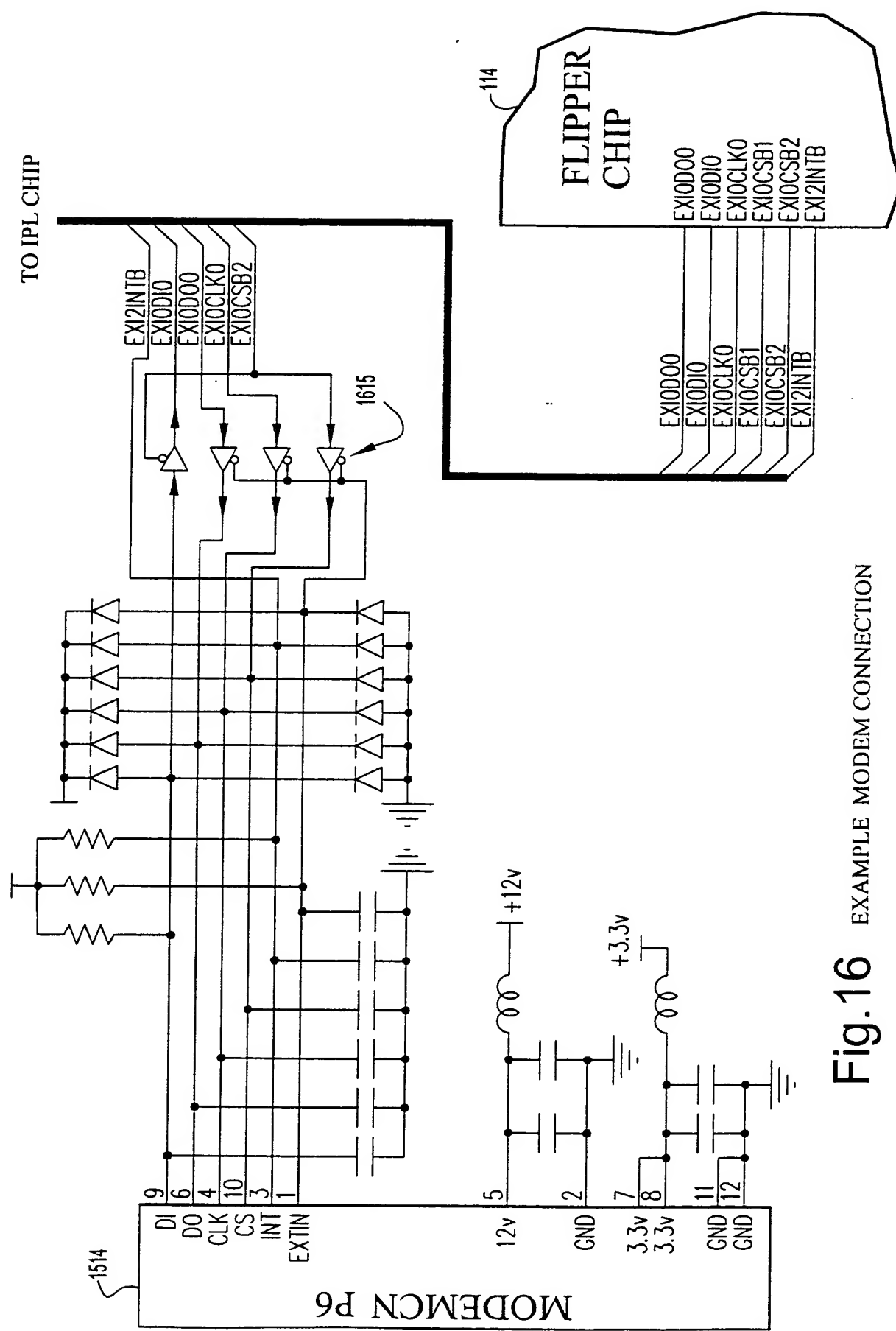


Fig.16 EXAMPLE MODEM CONNECTION

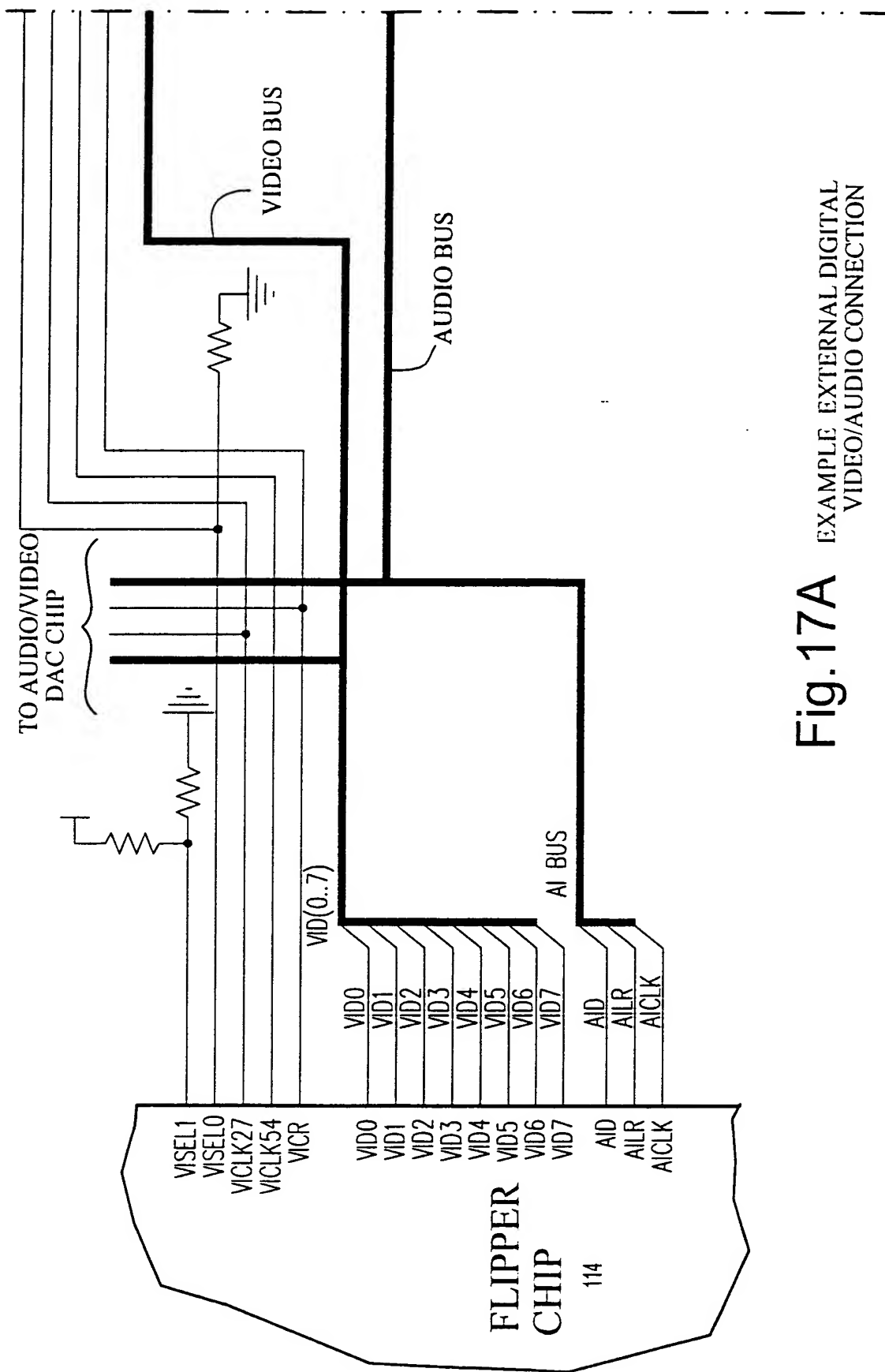


Fig.17A EXAMPLE EXTERNAL DIGITAL VIDEO/AUDIO CONNECTION

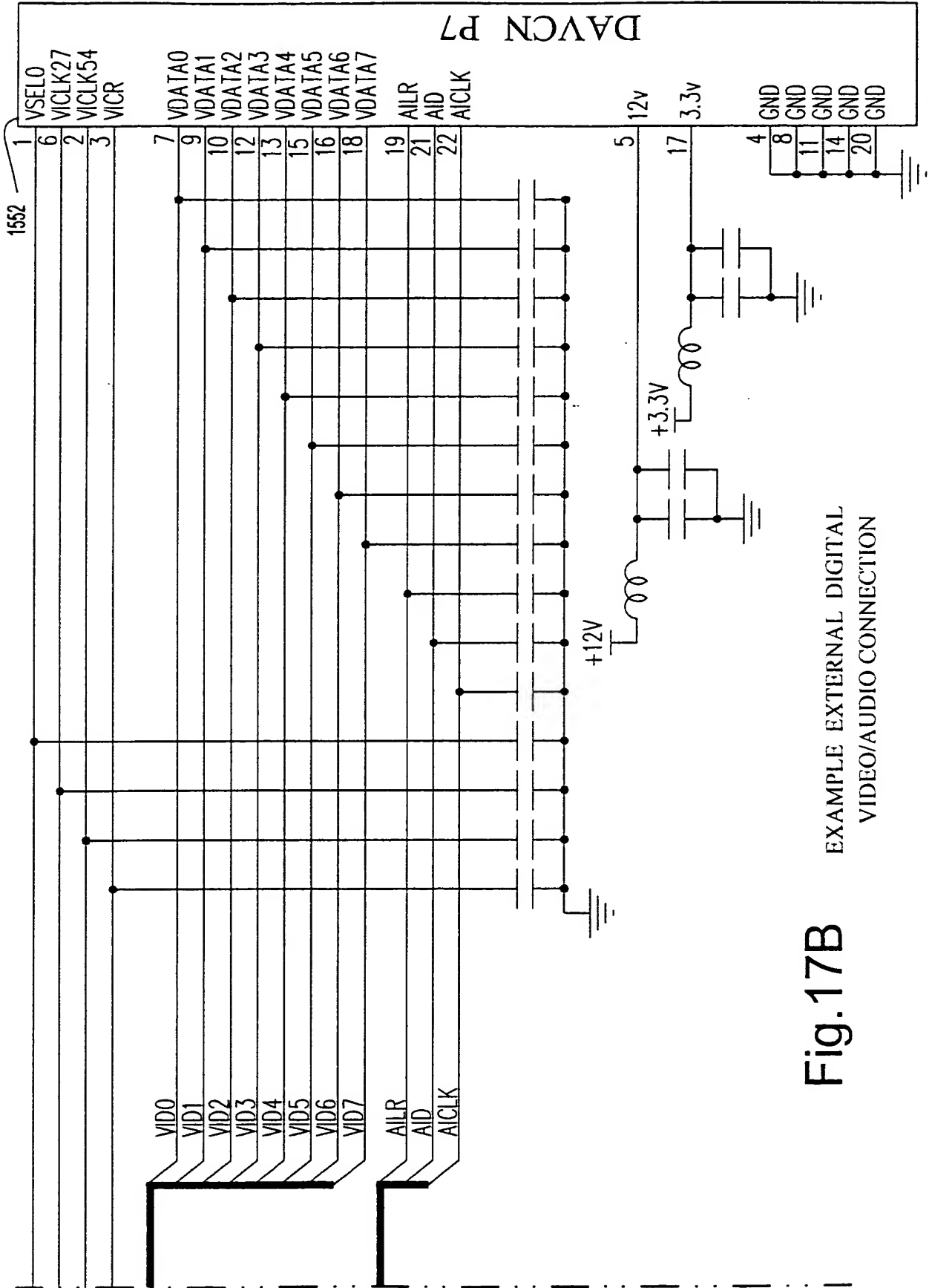


Fig.17B

EXAMPLE EXTERNAL DIGITAL
 VIDEO/AUDIO CONNECTION

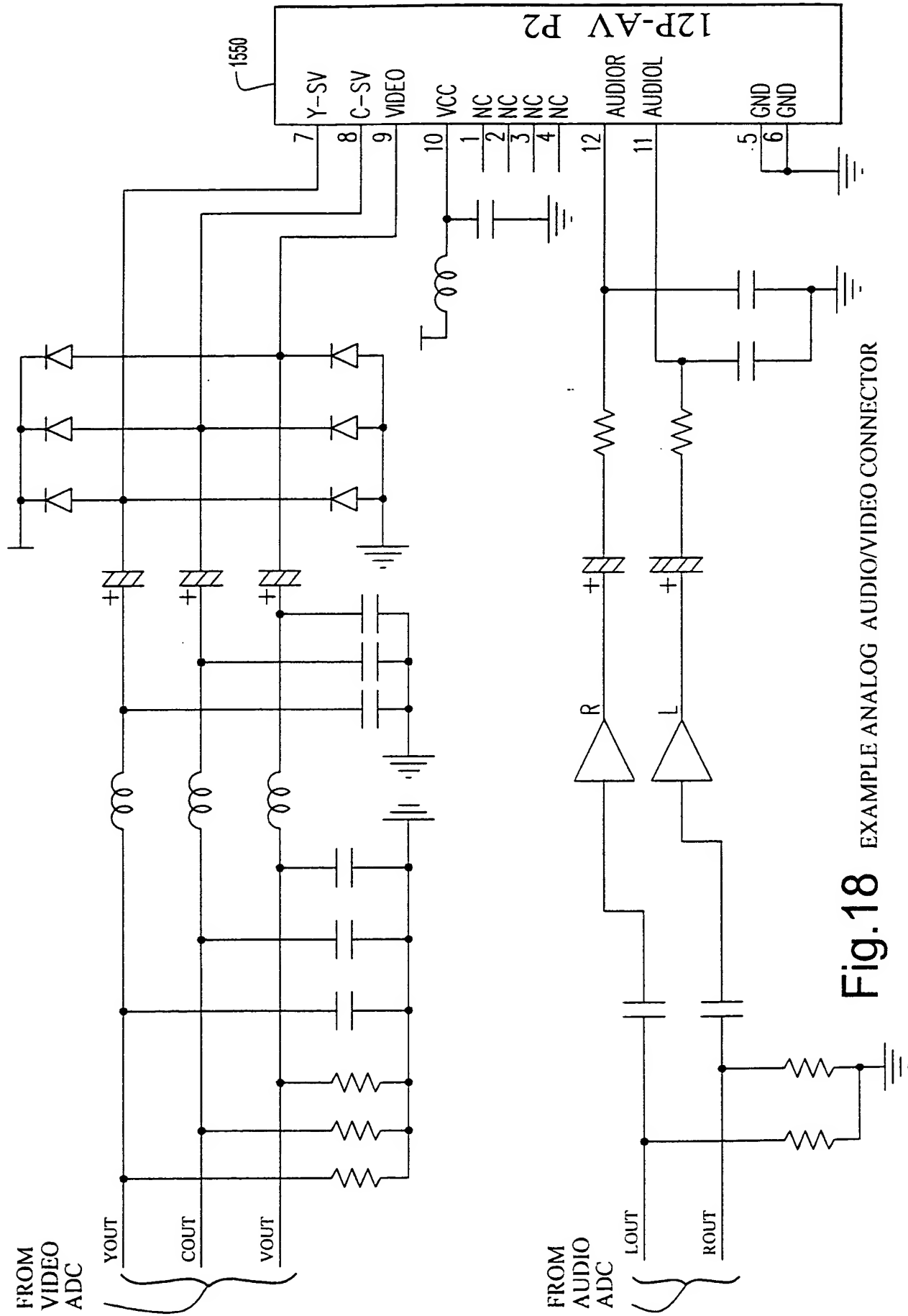


Fig.18 EXAMPLE ANALOG AUDIO/VIDEO CONNECTOR

Fig. 19A

EXAMPLE SDRAM EXPANSION CONNECTION

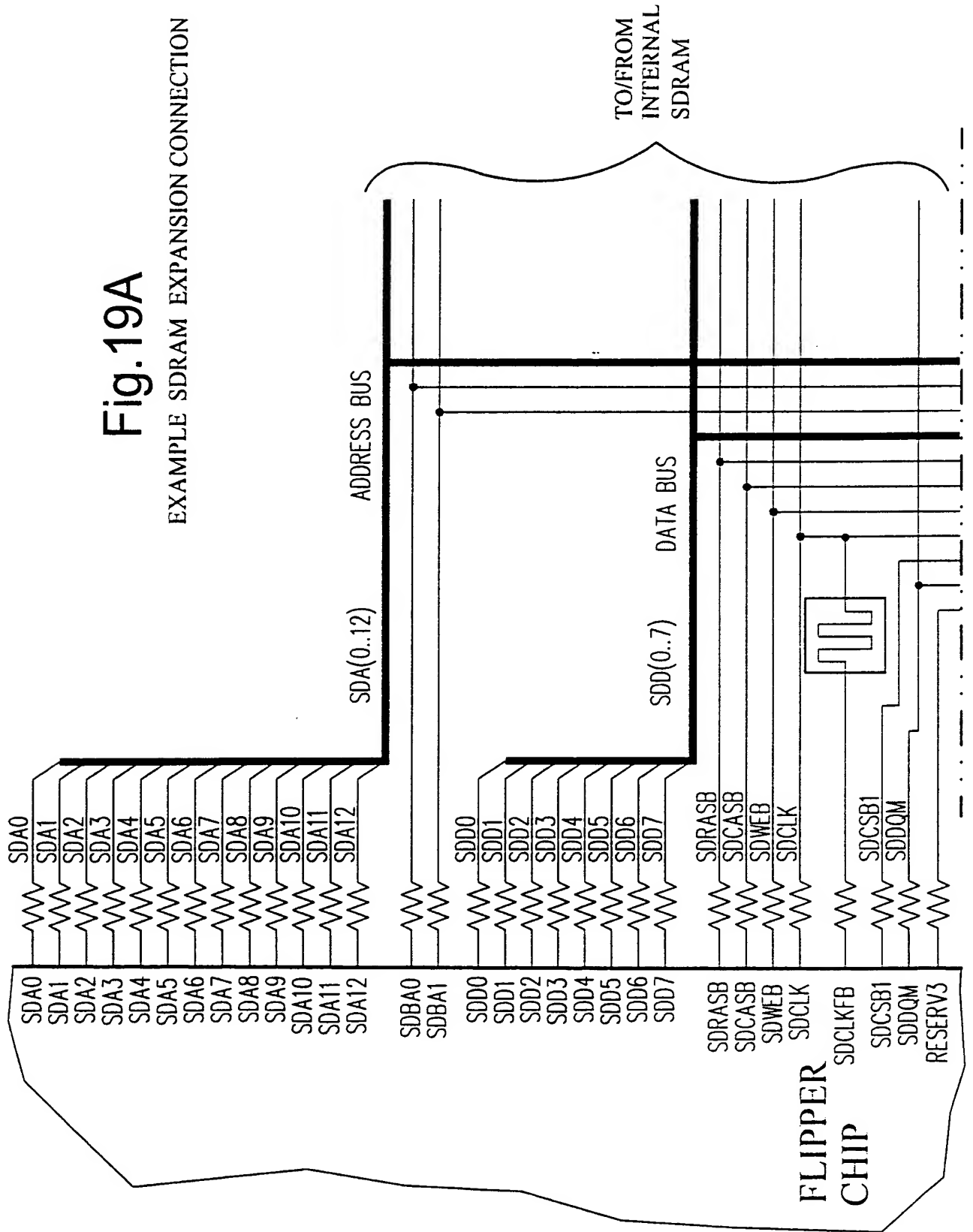
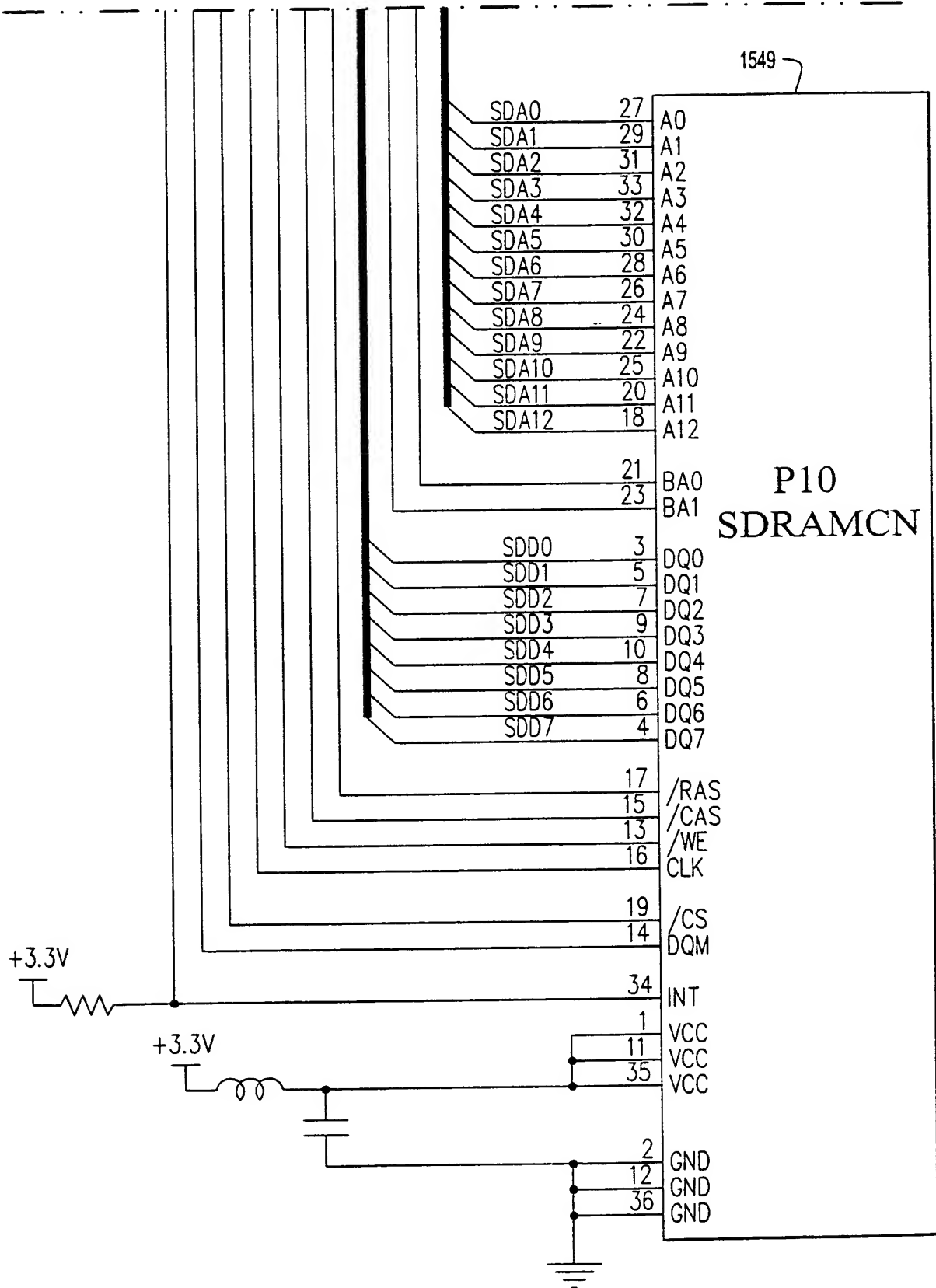


Fig.19B



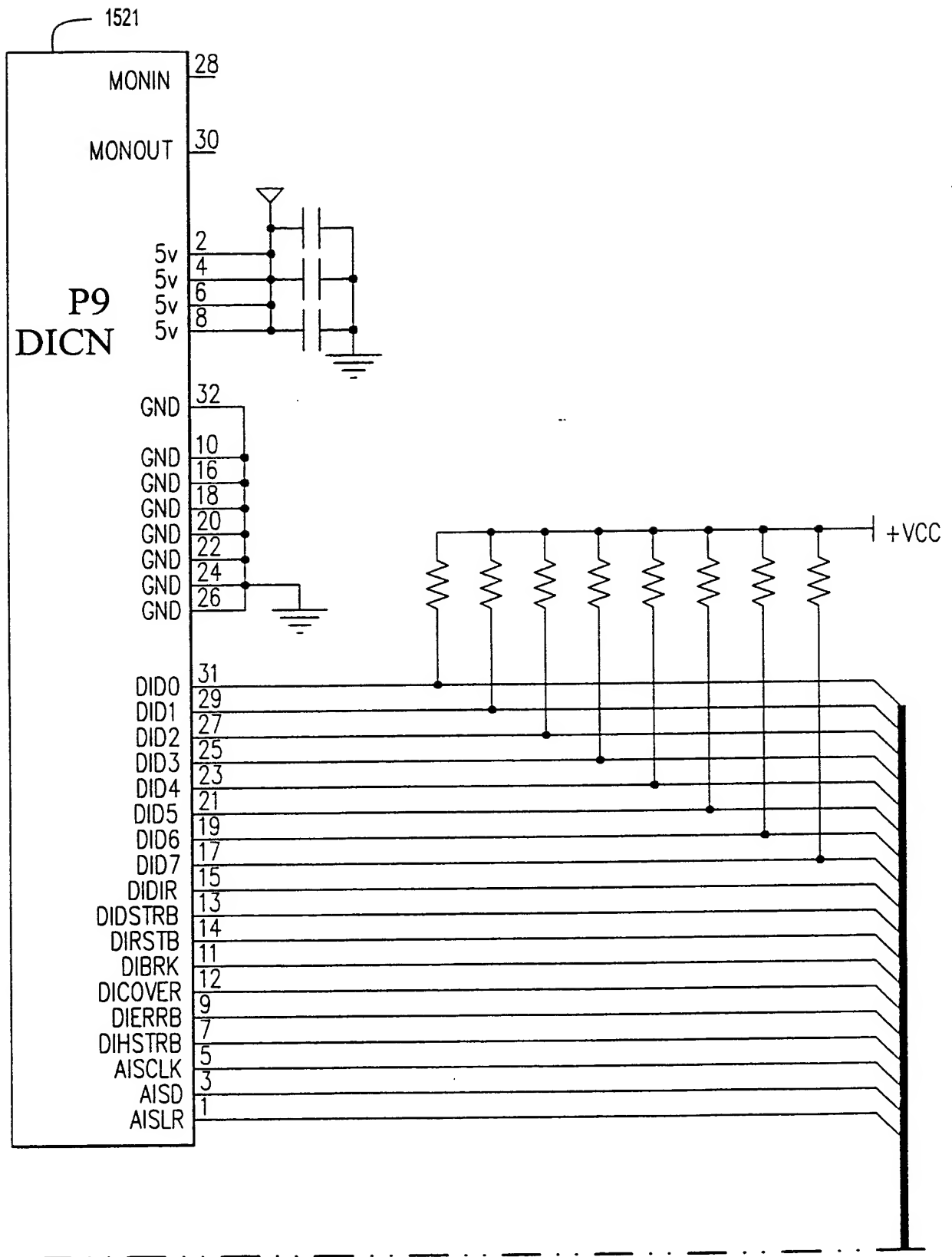


Fig.20A EXAMPLE DISK DRIVE CONNECTION

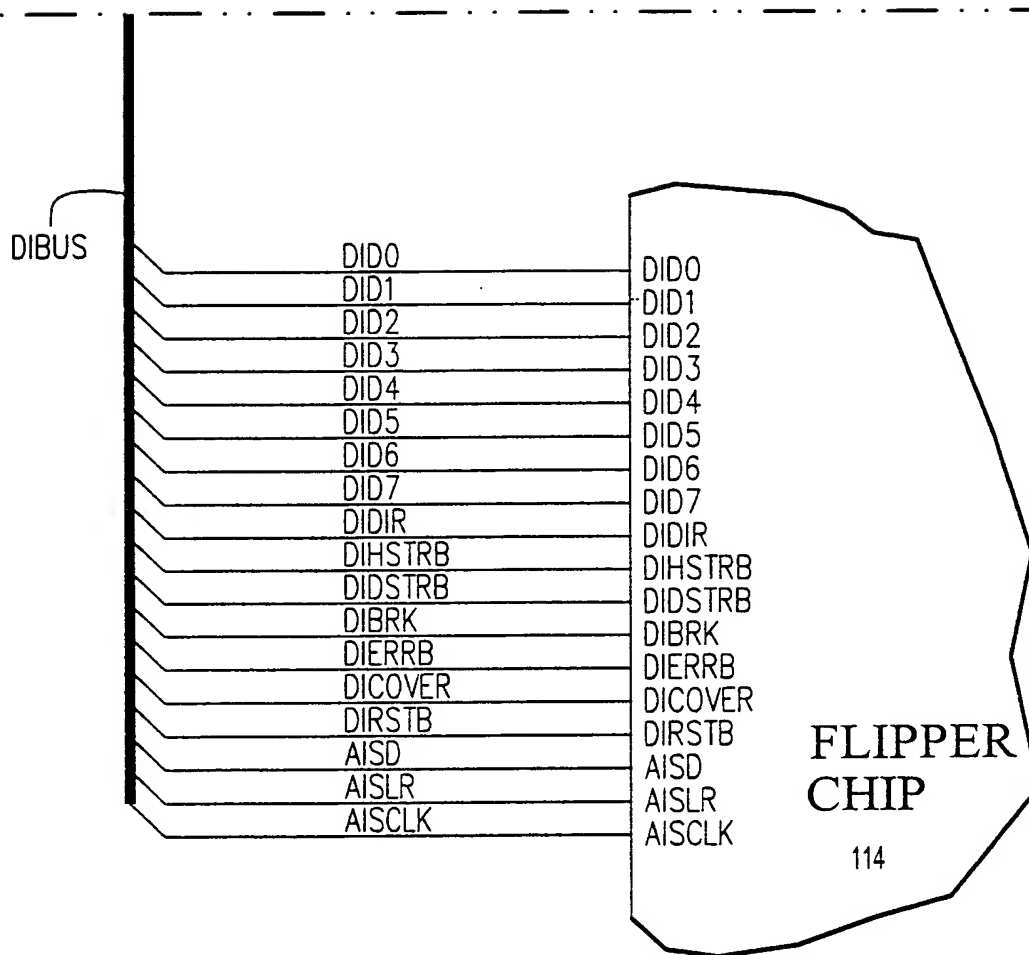


Fig.20B

EXAMPLE DISK DRIVE CONNECTION

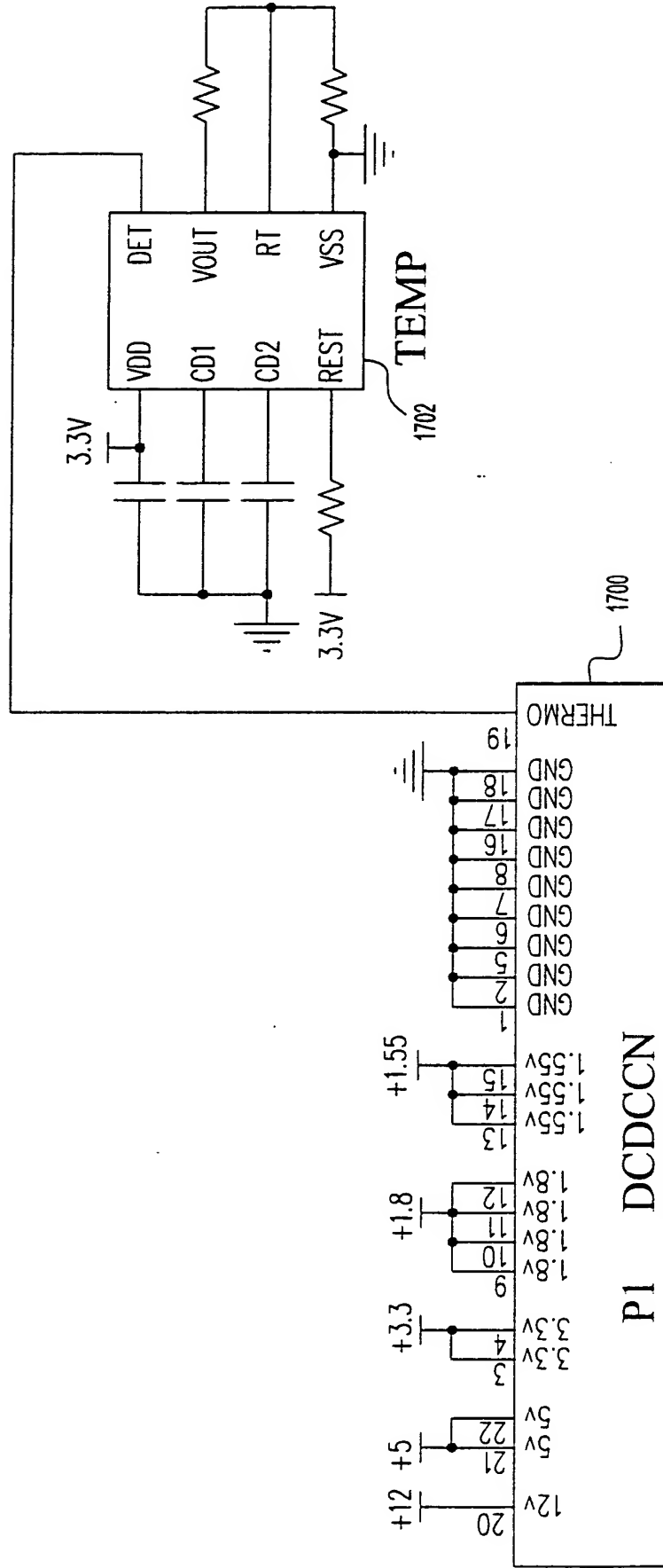


Fig.21 EXAMPLE POWER SUPPLY CONNECTION

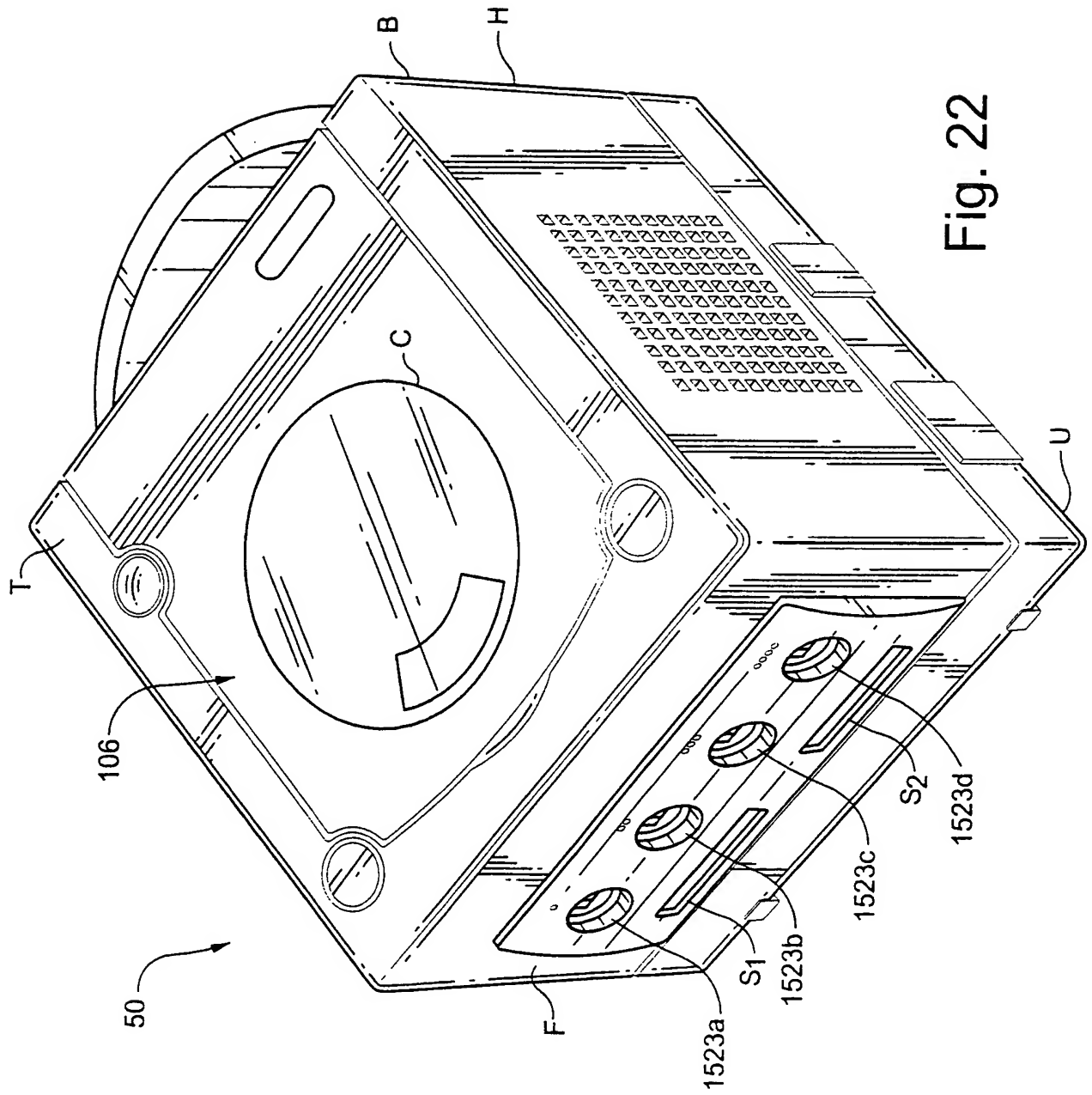


Fig. 22

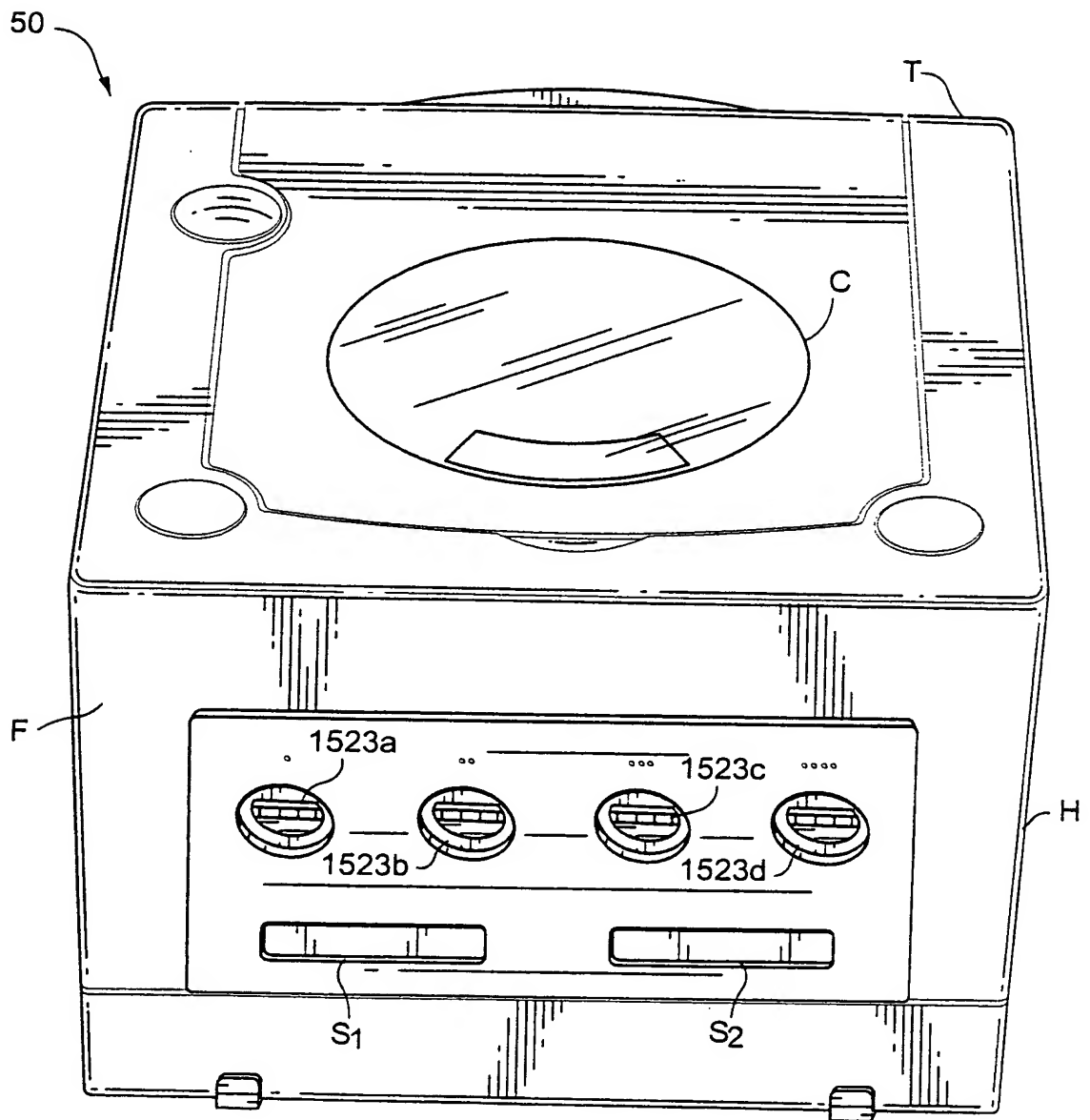


Fig. 23

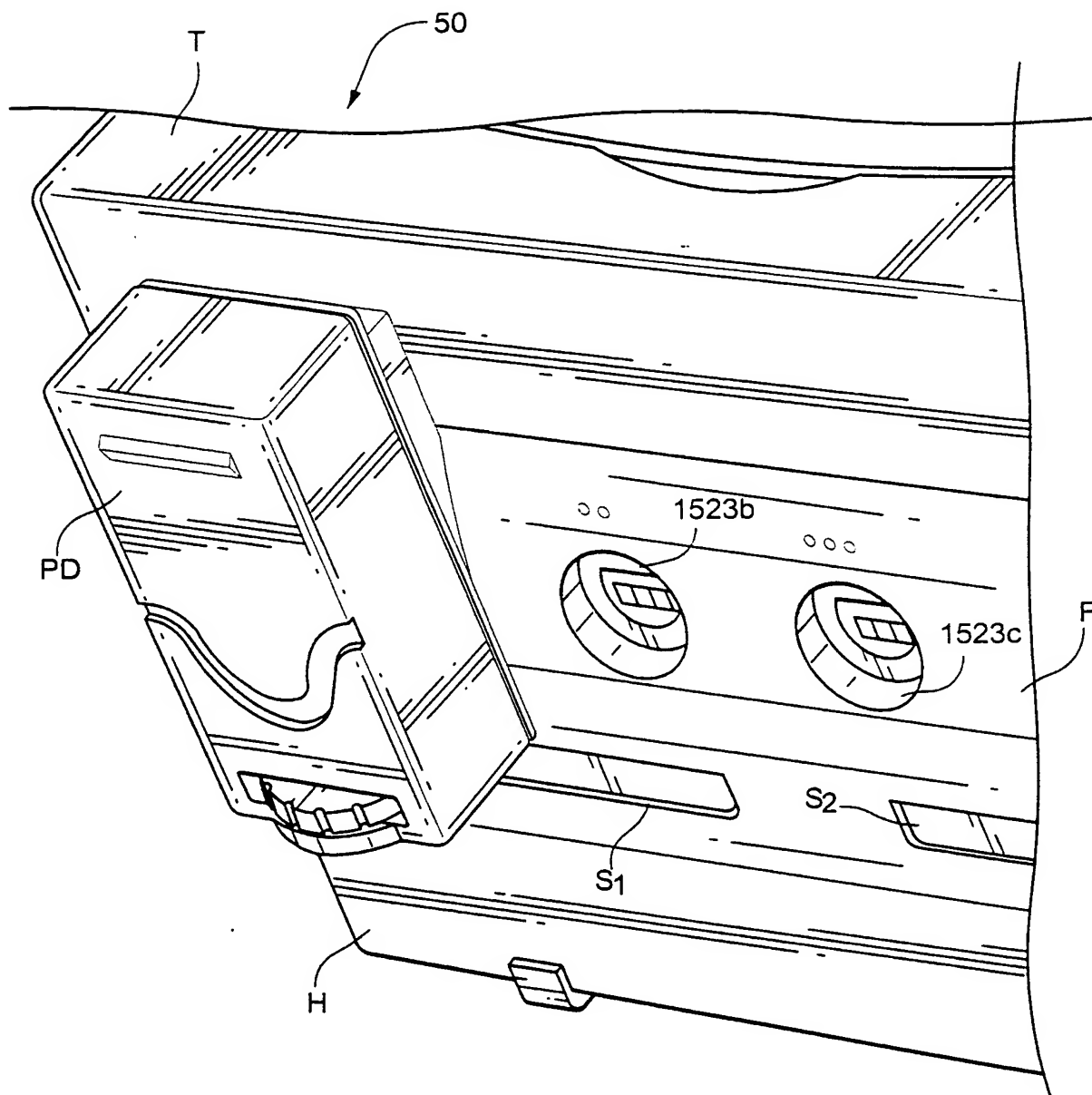


Fig. 24

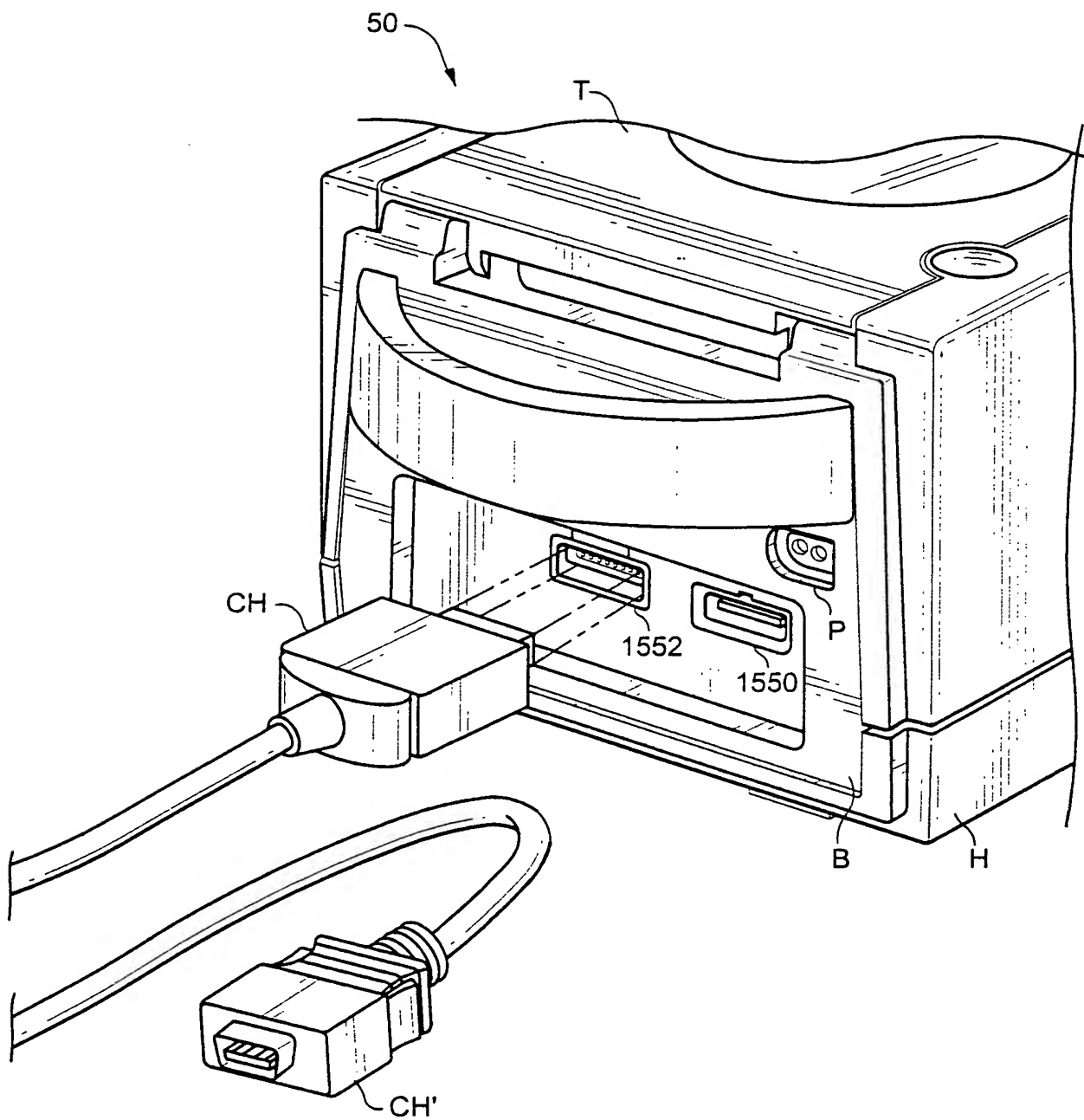


Fig. 25

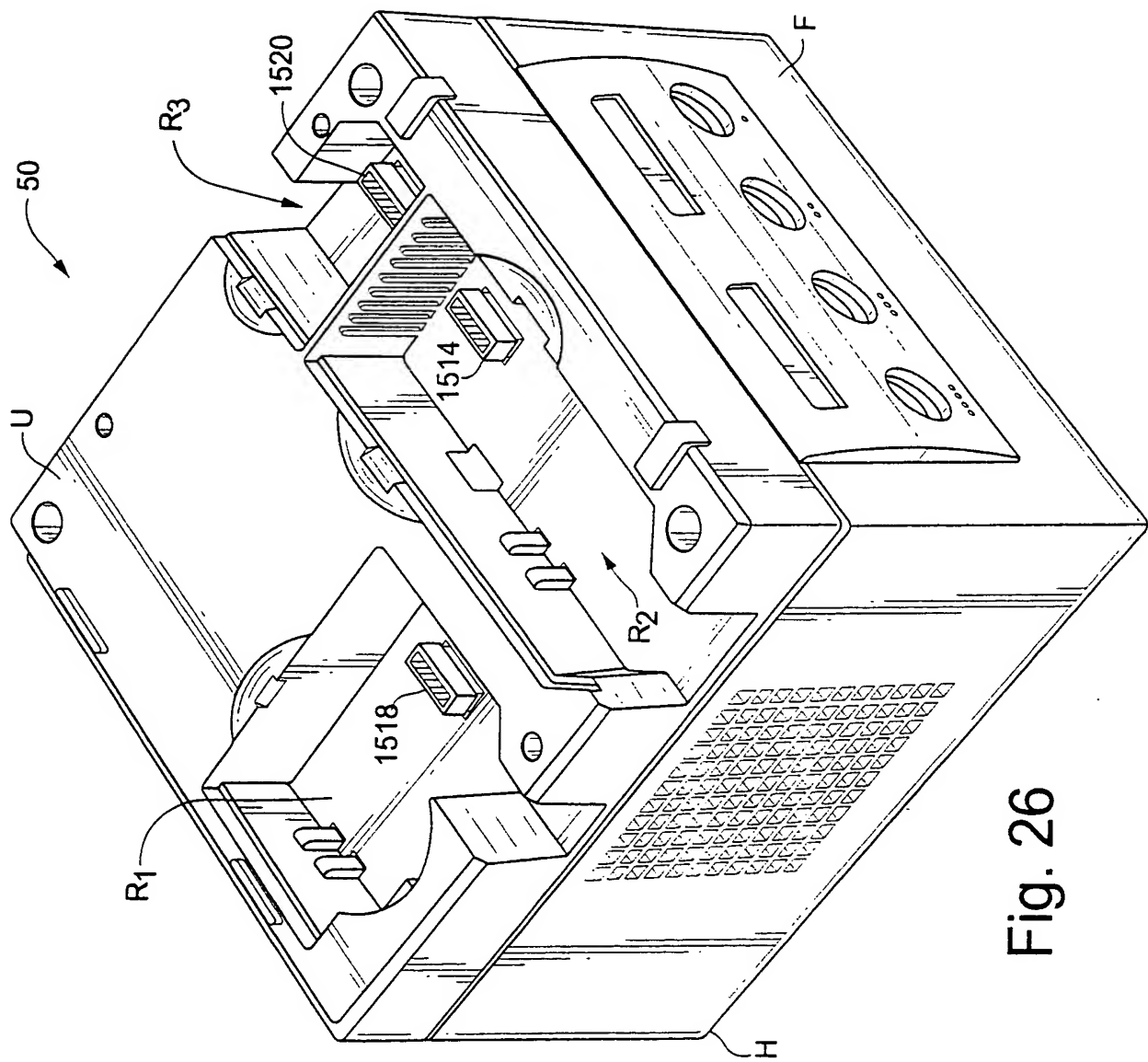


Fig. 26

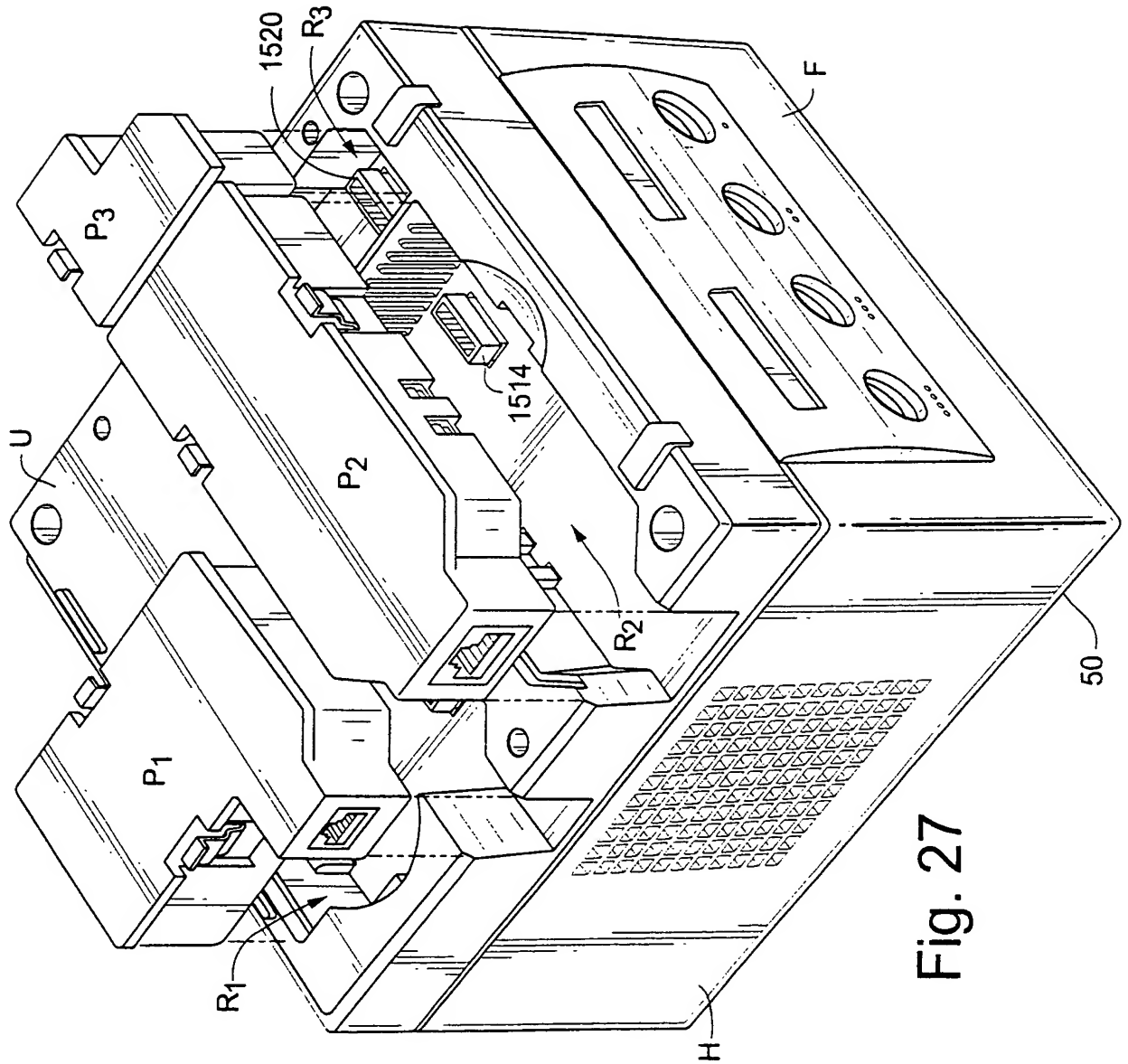
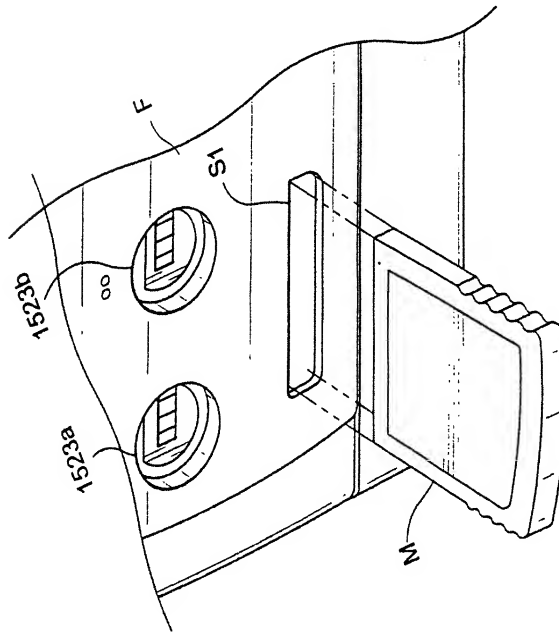
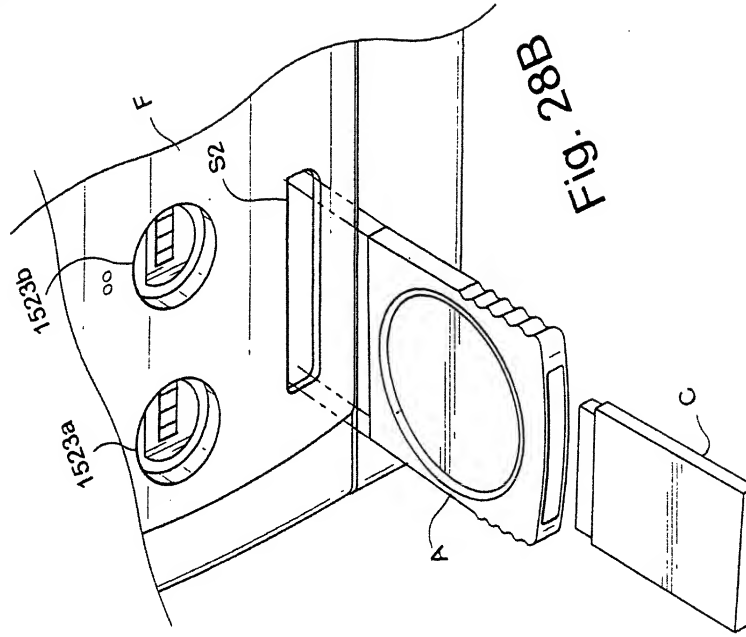


Fig. 27



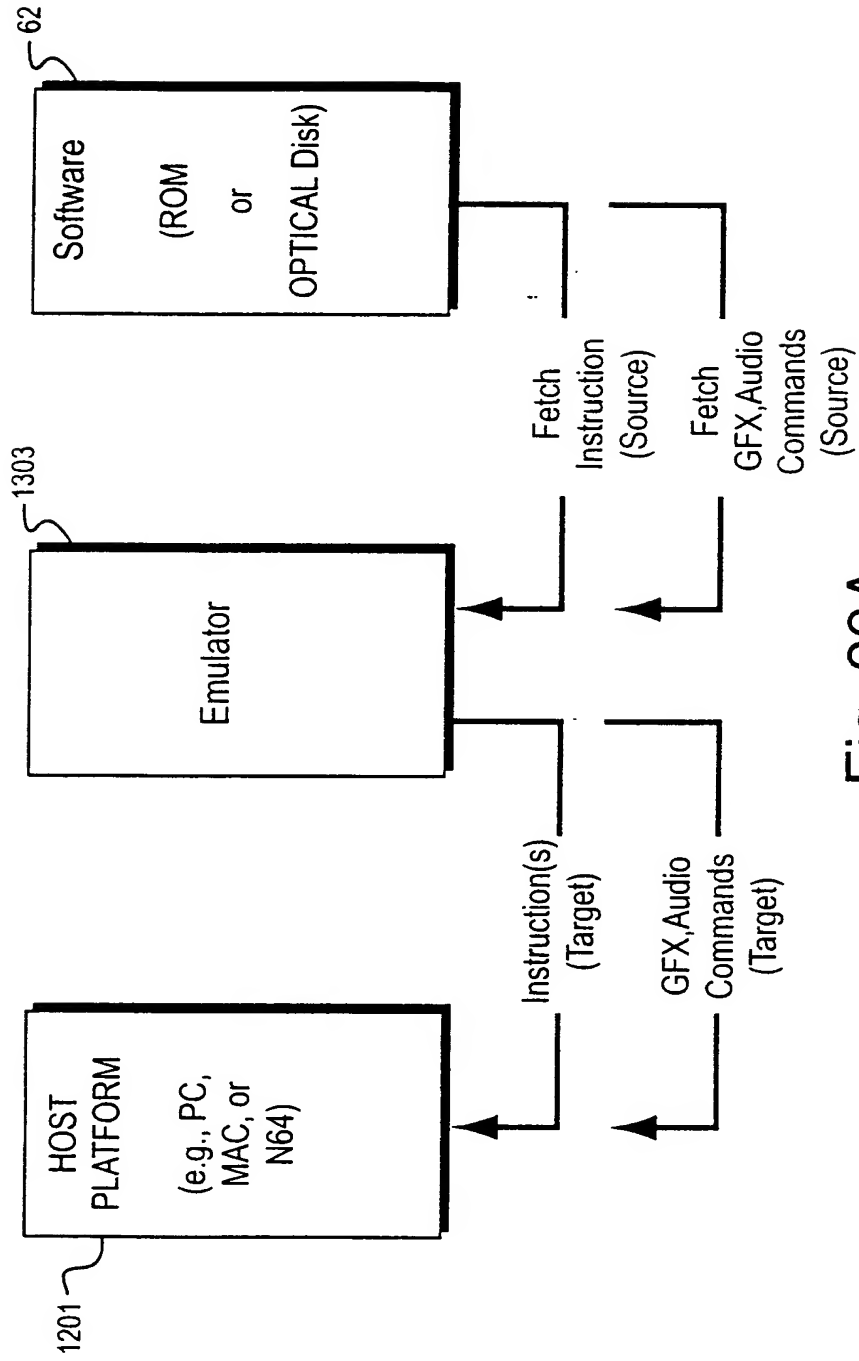


Fig. 29A

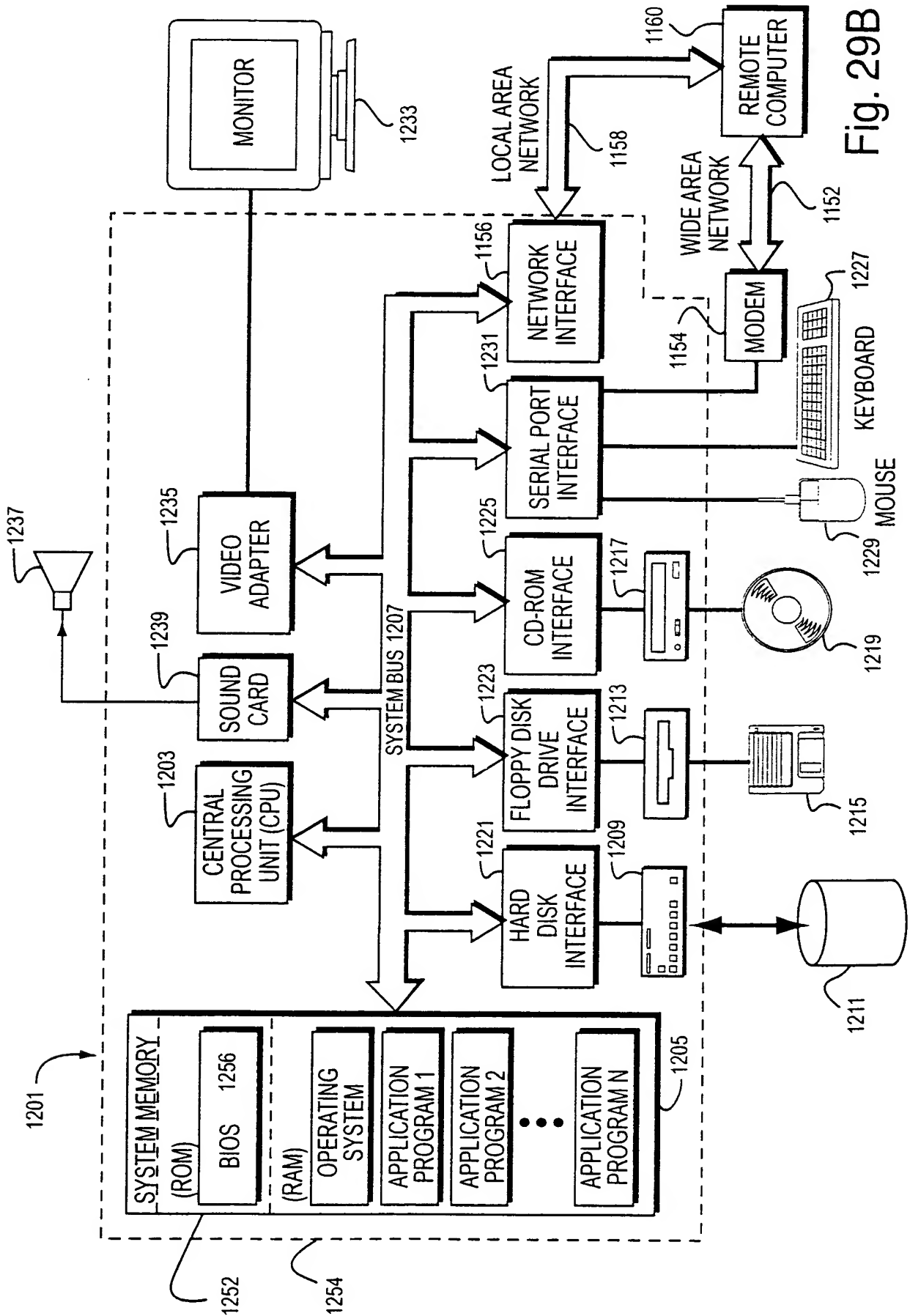


Fig. 29B